

# Aries-V6 VME / VXS

Extreme Signal Acquisition  
and FPGA-based Processing  
Without Compromise



## Features

## Benefits

Ten 16-bit ADCs at 250 MSPS with 500 MHz input bandwidth	Highest channel count available in a 6U slot
Three large pin count (1759-pin-package) Xilinx Virtex®-6 devices available per board (LX240, SX315, or SX475). Other configurations available	FPGA processing resources to match application requirements
Sample-accurate trigger input	Supports coherent processing of a large number of channels across multiple cards
Five GB DDR3 SDRAM memory	Large memory resources for application flexibility
Two fully independent banks (72 Mb/bank) of QDRII+ memory on backend FPGA	Random access memory available if needed
Single front panel clock input	Simplifies external clock distribution
Network interconnect through front panel SFP+ link, VITA 41.6 backplane and P2 RTM	Supports control plane via Gigabit Ethernet with all types of VME and VXS backplanes
Twelve fiber optic interfaces running at up to 6.4 Gb/s using CXP front panel connection	Flexible data movement across the front panel for use in standard VME environments
Advanced temperature and current monitoring	Protection from damage and usable in customer applications
Comprehensive developer's kit provided including FPGA interface cores, QuiXstart FPGA utilities, software and reference designs	Faster application development
Convection or conduction cooled options	Ruggedization designed in for demanding deployed applications

## Overview

The QuiXilica Aries-V6 VME / VXS is a 6U VME and ANSI/VITA 41 (VXS) compliant high-speed digitizer board that combines high density FPGA processing with ten 16-bit Analog Devices AD9467 ADC devices, with rates up to 250 MSPS.

By employing three Xilinx Virtex-6 FPGAs, Tekmicro's Aries-V6 combines ultra wideband signal acquisition with onboard high density FPGA processing. The result is a single slot solution that utilizes the latest ADC technology, supports advanced signal processing of up to 5.0 GB/s of digitized data, and forwards the results through a VME, RACE++, VXS or front panel connection to the next processing stage.

Aries-V6 enables multi-channel signal acquisition systems with direct sampling of up to 125 MHz of bandwidth to an upper bandwidth of 500 MHz for under-sampling applications. Signal processing is performed by three Xilinx Virtex-6 FPGAs, providing up to 6,048 DSP slices and 7.2 TeraMAC/s of processing for front-end DSP.

The Aries-V6 features high bandwidth, low latency interconnect paths between its FPGAs. These have been carefully specified to ensure that data from all ADC inputs can be combined and processed together within the onboard FPGA resources to support low-latency multi-channel applications such as adaptive beamforming using either the front end FPGAs or the back end FPGA.

Sample-accurate synchronization of ADC sampling on a single board, and between multiple boards, is done using an external trigger signal. This offers significant advantages in terms of channel matching performance for a range of advanced processing algorithms including multi-channel algorithms found in applications such as direction finding, STAP RADAR (Space Time Adaptive Processing) , EW, ELINT and SAR (Synthetic Aperture Radar) Image Formation.

The Aries-V6 is available for a wide range of operating environments including commercial grade, rugged air cooled and conduction cooled to support deployed applications such as unmanned airborne, naval and ground vehicles. For more details see Tekmicro's Ruggedization Data Sheet.

In addition to Aries-V6, Tekmicro offers a broad range of FPGA-based streaming I/O and FPGA processing solutions for both analog and digital I/O in a range of form factors.

## Aries-V6 VME / VXS Details

### ADC

Aries-V6 contains ten AD9467 16-bit 250 MSPS ADCs. The inputs are single-ended, AC coupled with a full scale input level of +12 dBm into 50  $\Omega$ .

### Virtex-6 FPGAs

Xilinx Virtex-6 FPGAs are the heart of the Aries-V6. The FPGAs interface between the ADC's, memory and I/O resources to provide a platform for implementing high performance real time processing. The Aries-V6 is configured with three high pin count Xilinx Virtex-6 devices (LX240, SX315, or SX475) per board. Other device types can be used optionally or mixed for custom configurations. All FPGAs are interconnected by wide parallel LVDS busses and via high speed serial links using the Xilinx GTX transceivers.

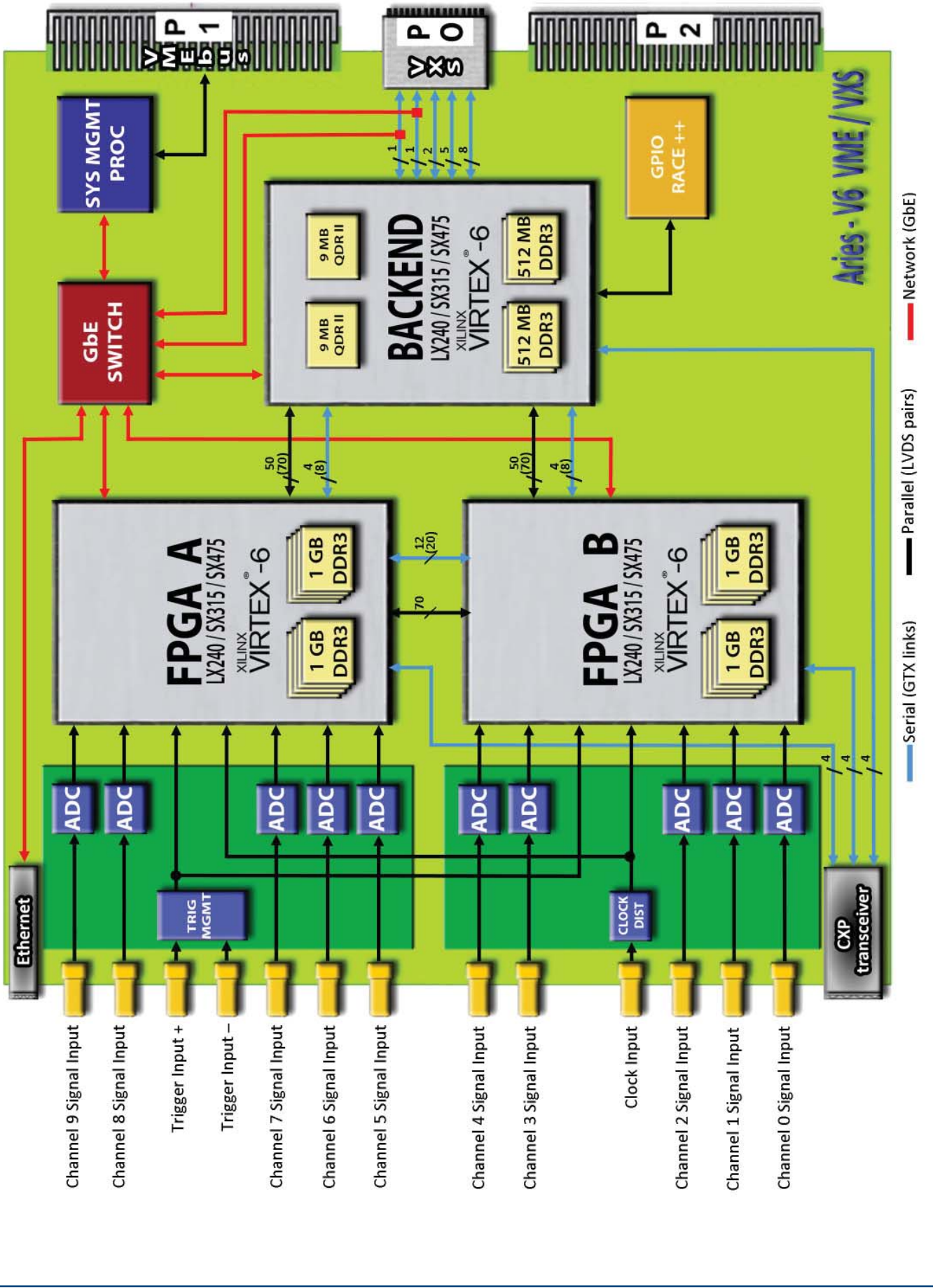
### Front Panel High Speed Serial I/O

One 12-fiber CXP site is provided on the front panel for standard protocols such as Gigabit Ethernet, Serial FPD (ANSI/VITA 17.1 & 17.2), and Fibre Channel. CXP modules and breakout cables are optionally available for flexible I/O capability.

### On-Board Gigabit Ethernet Networking and Switching

An on-board Gigabit Ethernet switch connected to each FPGA supports routing of control plane signaling and minimizes FPGA involvement for data distribution/forwarding between FPGAs. A dedicated SFP port which supports both fiber and copper Gigabit Ethernet connections is available to connect to an outside network.

# Aries-V6 Configurations



## VXS Backplane High Speed Serial I/O

The Aries-V6 can be used as a VITA 41.0 payload card. Up to eight high speed serial links of up to 3.125 Gb/s full duplex data rates are supported via VITA 41.0 MultiGig RT2 P0 connector. Custom or standard communication protocols can be run over these links by providing appropriate firmware in the FPGA.

## QuiXstart FPGA Configuration

A number of options are available for configuring the FPGA on the Aries-V6. A JTAG connection is available to allow users to configure the FPGA via standard Xilinx development tools. Onboard flash is available and can configure the FPGA on power up. Tekmicro's QuiXstart tool supports flexible configuration of the FPGA through a Gigabit Ethernet link from a remote server after a power up or reset event.

## Trigger

Trigger input connections are provided on the front panel to allow the hardware to be employed in a variety of radar and EW scenarios. The trigger inputs are LVDS (LVPECL is a factory build option). The trigger inputs may be used to synchronize multiple Aries-V6 boards to within a single sample period.

## Clock

One clock input serves all ADC devices. The minimum input clock level is 4.5 dBm into 50  $\Omega$ .

## Memory

The Aries-V6 has two independent banks of onboard DDR3 SDRAM for each FPGA. The front end FPGAs have two 1 GB banks, each with throughput of 6.4 GB/s, while the back end FPGA has two 512 MB banks, each with throughput of 3.2 GB/s. The total memory capacity is 5 GB with aggregate throughput of 32 GB/s across six banks. All DDR3 memory banks are clocked at 400 MHz for an 800 MT/s transfer rate. In addition, there are two fully independent banks of QDRII+ SRAM memory for the back end FPGA. Each QDRII+ device has a 72 Mbit capacity (144 Mbit total) supported by an 18 bit data bus per bank.

## System Monitoring / Damage Protection

The Aries-V6 includes facilities to monitor current and temperature at various points on the board. Current monitoring of all main power rails is available through the use of a Spartan6 FPGA. Die temperature monitoring of the three FPGAs and temperature monitoring of three locations on the PCB is also available. This allows a first level of protection when the Aries-V6 is operating in different environmental scenarios. The output from the sensors is available to users' FPGA firmware applications, to allow the user application to adapt to changes in environmental conditions. The Aries-V6 also uses the system monitoring sensors to implement a system protection mechanism which will, independently of the users' application, prevent excessive current or temperature from damaging the board.



# PERFORMANCE SPECIFICATIONS

## A/D Converter

**Quantity:** 10

**Sampling Rate:** Up to 250 MSPS

**Resolution:** 16 bits

**Type:** AD9467 from Analog Devices

**Bandwidth:** Up to 500 MHz

## Front Panel Analog Signal Input

**Quantity:** 10 ADC SSMC Connectors

**Type:** Single ended AC coupled

**ADC Full Scale Input:** +12 dBm into 50  $\Omega$  full scale

## Front Panel Trigger Inputs

**Quantity:** 1 via 2 SSMC Connectors

**Type:** 100  $\Omega$  differential terminated

Includes support for LVDS (LVPECL as factory build option)

**Mode:** Single common trigger for ADCs

## External Clock

**Quantity:** 1 SSMC Connector

**Type:** Single-ended AC coupled 50  $\Omega$  terminated

**Input Power Range:** 4.5 dBm (min) to +11 dBm (max)

**Operating Modes:** Single common clock distributed to ADCs

## Front Panel High Speed Serial Interface

12 Fiber Optic Transceivers on CXP module

Up to 6.4 Gb/s, 8B/10B or 64/66 encoding

Range of standard protocols, including Gigabit Ethernet and Serial FPDP.

## Network Interface

Front panel SFP for fiber or copper Gigabit Ethernet

VITA 41.6 P0 interface for 1000 BASE-KX Gigabit Ethernet.

Onboard Gigabit Ethernet switch

## MTBF

**Per MIL-HDBK-217:** 176,533 hours, Ground Benign environment

## JTAG Port

Access to Virtex-6 FPGAs is available via a custom JTAG cable assembly that interfaces with the standard Xilinx JTAG programming cable.

## Memory

**DDR3 SDRAM** (2 fully independent banks per FPGA)

**Size:** 1 GB per front end bank, 512 MB per back end bank

**Bus Width:** 64 bits per front end bank, 32 bits per back end bank

**Speed:** 400 MHz clock rate, 800 MT/s

**QDRII+ SRAM** (2 fully independent banks for back end FPGA)

**Size:** 72 Mbits per bank (144 Mbits total)

**Bus Width:** 18 bits per bank

**Speed:** Up to 500 MHz clock rate

## Backplane I/O

**VME Interface:** A32:D32 slave interface

**VXS Interface:** P0 connector supports 8X high speed serial links on the backplane

**GPIO Interface:** P2 connector

**RACE++ Interface (Optional):** P2 Connector can be configured to support RACE++ environments

**Rear Transition Module (Optional):** For rear access to the board, a Rear Transition Module is available which provides connections for GPIO connections, network access, PPS, and trigger signals

## Size

Standard ANSI/VITA 1.1-1997 (R2003) VMEbus board, 6U x 4HP, single 0.8" slot

Optional VXS P0 connector for backplane I/O

## Power

+5V, +3.3V,  $\pm$ 12V from backplane. Power consumption is dependent on customer application. Power estimation model is provided as part of the Developers Kit.

Contact factory for additional performance details.



## Environmental / Ruggedization

In addition to providing high performance, Tekmicro boards and systems have been designed for ruggedization and power management. Tekmicro products operate effectively in laboratory, rugged air-cooled and rugged conduction-cooled environments to meet the needs of deployed applications.

## Ruggedization Options

Specification	Commercial	Rugged Level 2	Rugged Level 3
<b>Cooling</b>	Convection	Convection	Conduction
<b>Operational Temperature</b>	0 to +55 °C (300 LFM airflow)	-40 to +70 °C (600 LFM airflow)	-40 to +85 °C (At Card Edge)
<b>Storage Temperature</b>	-40 to +85 °C	-55 to +100 °C	-55 to +125 °C
<b>Relative Humidity</b>	10% to 95% non-condensing	5% to 95% non-condensing	0% to 95% non-condensing
<b>Conformal Coating</b>	No	Yes	Yes
<b>Shock</b>	½ sine pulse, 20 g, 11 ms	½ sine pulse, 20 g, 11 ms	½ sine pulse, 40 g, 11 ms
<b>Vibration (Sine)</b>	2 g peak 15 to 2,000 Hz	10 g peak 15 to 2,000 Hz	10 g peak 15 to 2,000 Hz
<b>Vibration (Random)</b>	0.003 g <sup>2</sup> /Hz from 15 to 2,000 Hz	0.04 g <sup>2</sup> /Hz from 15 to 2,000 Hz	0.1 g <sup>2</sup> /Hz from 15 to 2,000 Hz



TEK Microsystems, Inc.  
 300 Apollo Drive  
 Chelmsford, MA 01824  
 voice: +1.978.244.9200  
 fax: +1.978.328.5951  
 email: sales@tekmicro.com  
 web: www.tekmicro.com