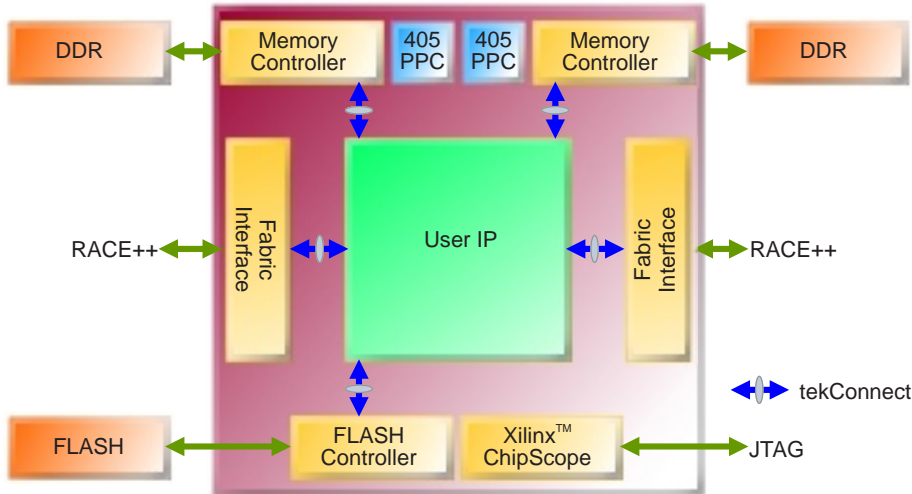


Standard FPGA Configuration



Products Supported:

PowerRACE-3

Interconnect:

tekConnect v1.1 64 bit data path, half or full duplex
Simple FIFO interface with flow control
Supports raw or framed/packetized data streams
Supports event messaging

Supplied Cores:

Fabric Interface tekConnect interface to RACE++ port
Master/Slave RACE++ interface
Integrated DMA controller
Throughput up to 267 MB/s

Memory Controller tekConnect interface to DDR SDRAM
32-bit memory data path at 125 MHz
Throughput up to 1.0 GB/s

FLASH Controller tekConnect interface to FLASH memory

Xilinx™ Chipscope Internal Logic Analyzer to support hardware debug through JTAG port

Toolchain:

Synthesis:
Xilinx ISE 6.2i
Synplicity Symplify Pro 7.5

Simulation:
Mentor Graphics ModelSim SE

Place & Route:
Xilinx ISE 6.2i

Programming:
tekX software (through local processor)
Xilinx JTAG cable

Features

tekConnect Open Interconnect Definition:

- Provides modular, uniform interface to all Tekmicro IP cores, simplifying custom IP development
- Preserves IP investment for future products and fabrics

Factory FPGA Image with Demo Software Application:

- Provides out-of-the-box operation to jump start development
- Provides ready-made, documented example

Comprehensive Suite of Off-the-Shelf IP Cores:

- Reduces development costs and risks
- Reduces time-to-market

Technical Support:

Knowledgeable, accessible, and friendly technical and applications support that assures customer success

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