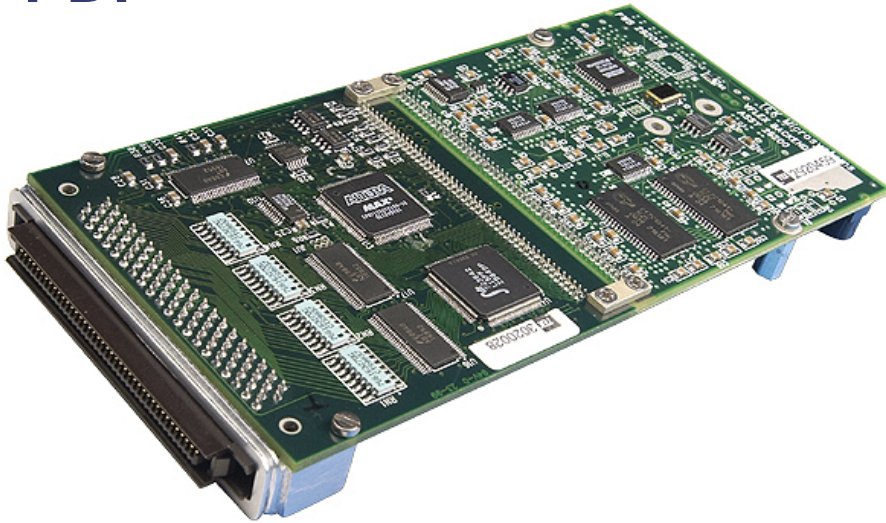


Parallel Transfer I/O Modules**FPDP**

Tekmicro's FPDP I/O module is recommended when a highly flexible ANSI/VITA 17 Front Panel Data Port (FPDP) interface is required. This module offers the capability to connect carriers via the front panel thereby lowering traffic on the backplane.

The physical interface supports software programmable selection of FPDP/TM, /R or /RM functionality, allowing a single module to act as a data transmitter or receiver under software control. The interface uses TTL signal levels for data and control signals and supports both TTL and PECL signal levels, selectable under software control, for the STROBE signal.

A customizable FPGA implements the FPDP control functions, allowing applications to easily support a wide range of functions for the optional FPDP PIO signals. Data words are buffered in a bidirectional FIFO memory, allowing the module to absorb extended host bus latencies without loss of data.

Cabling solutions are easily accomplished for this product using industry standard 80-pin connectors. Changing the direction of the FPDP bus is as easy as changing the value of a register and requires no physical contact with the module to add/remove jumpers or to reconfigure terminations.

Tekmicro's FPDP PMCs are fully compatible with the current generation of PMC-enabled VMEbus Single Board Computers. Tekmicro also offers turnkey solutions for RACEway and FPDP PMC users on its own PowerRACE and JazzStream I/O Controller and Processor Cards. Details of supported configurations can be found at www.tekmicro.com on the Host Support datasheet.

Integration Examples

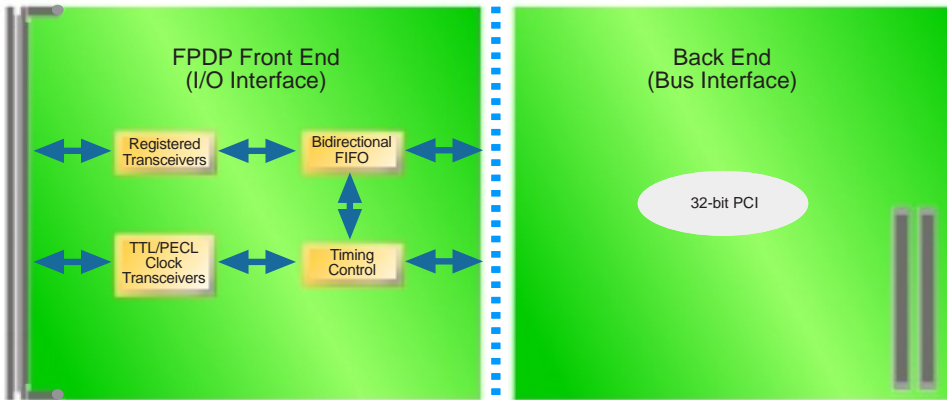
Direction-finding systems

SIGINT systems

Radar

Sonar

FPDP



I/O Connector:

80-pin FPDP connector

Features

Fully compliant with PCI 2.1 specification

Interoperable with supported hosts. Drop-in integration with RACEway and MC/OS using Tekmicro's PowerRACE carrier card.

TTL and PECL STROBE support

Supports older FPDP implementations as well as newer PECL technology

Onboard clock synthesizer

Supports exact generation of arbitrary output clock rates

Memory buffer

Allows zero wait state DMA block transfers; supports custom applications which require lookup or temporary memory

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Specifications:

Front End:

I/O Interface	ANSI/VITA 17 Front Panel Data Port (FPDP)
Word Width	32 bits
Clock Rate	DC to 20 MHz (TTL) DC to 40 MHz (PECL)
Burst Data Rate	160 MB/s
Sustained Data Rate	Up to full PCI bandwidth of 132 MB/s

Back End:

Bus Interface	32-bit, 33MHz PCI 2.1
Burst Rate Over Bus	160 MB/s
Sustained Throughput (max)	60-160 MB/s
Memory Capacity	1 MB buffer memory, 256K x 32
Interrupt Support	Programmable through FPGA
DMA Support	Two integrated linked-list DMA controllers

General:

Mechanical	Single-wide PMC module
Power Requirements	+5 Volts, 1300 mA
Operating Temperature	0° to +55°C (Commercial) -40° to +70°C (Rugged Level 2)
Storage Temperature	-40° to +85°C (Commercial) -55° to +85°C (Rugged Level 2)
Ruggedization	Available commercial grade and Rugged Level 2. See Tekmicro Ruggedization Data Sheet for definition of environmental performance specifications.
Warranty	One year limited hardware warranty Ninety day limited software warranty

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