QuiXilica family

Tekmicro

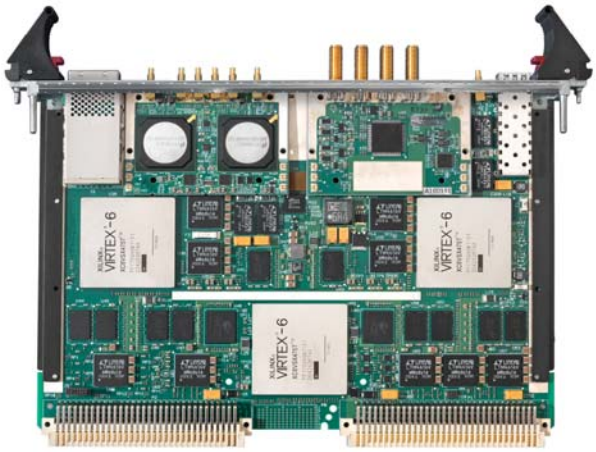
The Leader In FPGA-based Sensor I/O Processing

Gemini-V6 VME / VXS

Extreme Signal Acquisition

and FPGA-based Processing

Without Compromise



Features	Benefits
One 12-bit ADC at 3.6 GSPS, also supports three channels at 1.8 GSPS	Fastest 12-bit sampling in a COTS product and best available solution for 1st and 2nd Nyquist sampling with 900 MHz staring bandwidth
Combines ADC with DAC output channel at up to 4.0 GSPS	Intergrated solution for signal digitization and generation with low latency FPGA processing and DRFM buffering
Three Xilinx Virtex®-6 FPGAs	Acquisition, processing and generation on a single card without backplane throughput limitations
Sample-accurate trigger input	Supports coherent processing of a large number of channels across multiple cards
Five GB DDR3 SDRAM memory	Large memory resources for DRFM applications at full rate
Two fully independent banks (72 Mb/bank) of QDRII+ memory on backend FPGA	Random access memory available if needed
Single front panel clock input	Simplifies external clock distribution in many applications
Network interconnect through front panel SFP+ link, VITA 41.6 backplane and P2 RTM	Supports control plane via Gigabit Ethernet with all types of VME and VXS backplanes
Twelve fiber optic interfaces running at up to 6.4 Gb/s using CXP front panel connection	Flexible data movement across the front panel for use in standard VME environments
Advanced temperature and current monitoring	Protection from damage and usable in customer applications
Comprehensive developer's kit provided including FPGA interface cores, QuiXstart FPGA utilities, software and reference designs	Faster application development
Convection or conduction cooled options	Ruggedization designed in for demanding deployed applications

Overview

The QuiXilica Gemini-V6 VXS is a 6U VME and ANSI/VITA 41 (VXS) compliant high-speed digitizer board that combines high density FPGA processing with the latest 12-bit ADC and DAC technology. The Gemini-V6 supports either one input channel at 3.6 GSPS or three input channels at 1.8 GSPS, combined with a high speed output channel at up to 4.0 GSPS.

By employing three Xilinx Virtex-6 FPGAs, Tekmicro's Gemini-V6 combines high resolution wideband signal acquisition and generation with the onboard high density FPGA processing for a range of radar and Electronic Warfare applications such as target generation, jamming, and CM / CCM techniques. The result is a single slot solution that utilizes the latest ADC and DAC technology, supports advanced signal processing of up to 8+ GB/s of digitized data, and forwards the results through a VME, RACE++, VXS or front panel connection to the next processing stage.

Sample accurate synchronization of ADC sampling and DAC outputs on a single board, and between multiple boards, is done using an external trigger signal. This offers significant advantages in terms of channel matching performance for a range of advanced processing algorithms including multi-channel algorithms found in applications such as direction finding, STAP (Space Time Adaptive Processing) RADAR, EW, ELINT and Synthetic Aperture Radar (SAR) Image Formation.

The Gemini-V6 features high bandwidth, low latency interconnect paths between its FPGAs. These have been carefully specified to ensure that data from all ADC inputs can be combined and processed and then used to generate an appropriate DAC output.

The Gemini-V6 is available for a wide range of operating environments including commercial grade, rugged air cooled, and conduction cooled to support deployed applications such as unmanned airborne, naval and ground vehicles. For more details see Tekmicro's Ruggedization Data Sheet.

In addition to Gemini-V6, Tekmicro offers a broad range of Xilinx Virtex-6 based streaming I/O and FPGA processing solutions for both analog and digital I/O in a range of form factors.

Gemini-V6 VXS Details

ADC

The Gemini-V6 contains two ADC12D1800RF dual 12-bit 1.8 GSPS ADCs from National Semiconductor. One ADC device is used for analog input only, and one is used for analog and trigger inputs. Each ADC device is configurable as either a single channel of 3.6 GSPS digitization or two channels of 1.8 GSPS digitization, resulting in support of either one analog input at 3.6 GSPS or three analog inputs at 1.8 GSPS. The analog inputs are single-ended, AC coupled into 50 Ω.

DAC

The Gemini-V6 contains one MD653D 12-bit 4.0 GSPS DAC from Euvis. The DAC may be operated in Normal Hold (NH) or Return To Zero (RZ) mode and has a 4 GHz full power bandwidth. The analog output may be configured as either single-ended or differential as a build option with a full scale output of -4 dBm into 50 Ω.

Virtex-6 FPGAs

Xilinx Virtex-6 FPGAs are the heart of the Gemini-V6. The FPGAs interface between the ADC's, memory, DAC's and I/O resources to provide a platform for implementing high performance real time processing. The Gemini-V6 is configured with three high pin count Xilinx Virtex-6 devices (LX240, SX315, or SX475) per board. Other device types can be used optionally or mixed for custom configurations. All FPGAs are interconnected by wide parallel LVDS busses and via high speed serial links using the Xilinx GTX transceivers.

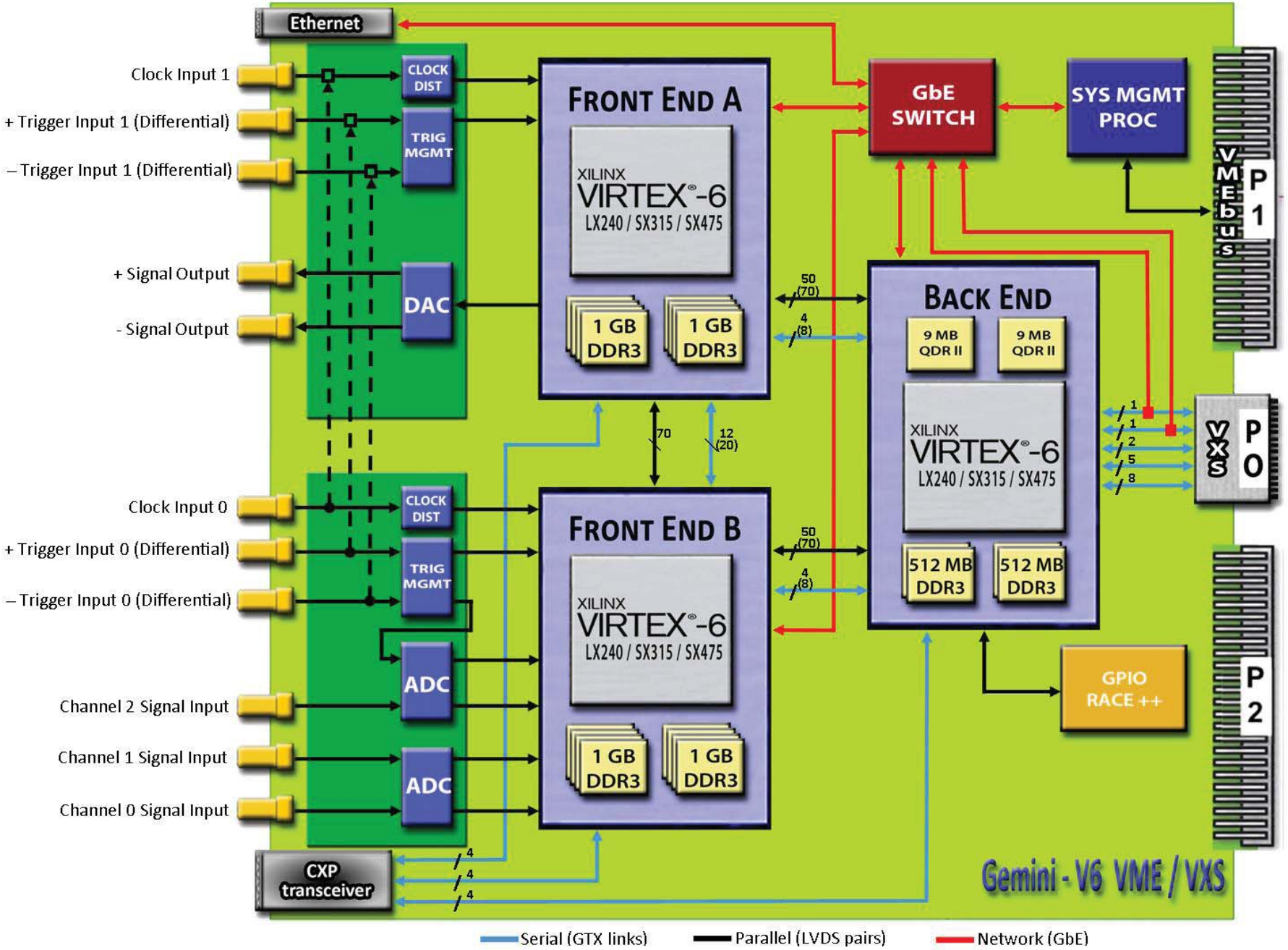
Front Panel High Speed Serial I/O

One 12-fiber CXP site is provided on the front panel for standard protocols such as Gigabit Ethernet, Serial FPDP (ANSI/VITA 17.1 & 17.2), and Fibre Channel. CXP modules and breakout cables are optionally available for flexible I/O capability.

VXS Backplane High Speed Serial I/O

The Gemini-V6 can be used as a VITA 41.0 payload card. Up to eight high speed serial links of up to 3.125 Gb/s full duplex data rates are supported via VITA 41.0 MultiGig RT2 P0 connector. Custom or standard communication protocols can be run over these links by providing appropriate firmware in the FPGA.

Gemini-V6 Configurations



QuiXstart FPGA Configuration

A number of options are available for configuring the FPGA on the Gemini-V6. A JTAG connection is available to allow users to configure the FPGA via standard Xilinx development tools. Onboard flash is available and can configure the FPGA on power up. Tekmicro's QuiXstart tool supports flexible configuration of the FPGA through a Gigabit Ethernet link from a remote server after a power up or reset event.

Trigger

Two Trigger inputs are provided on the front panel to allow the hardware to be employed in a variety of radar and electronic warfare scenarios. Each trigger input is differential, supporting LVDS, and LVPECL (as a build option). One trigger input is used for the ADC channels and the other is used for the DAC channel. The triggers are sampled at the ADC and DAC clock rates, respectively, providing sample-accurate synchronization both within a single Gemini-V6 card and across multiple cards in a system.

Clock

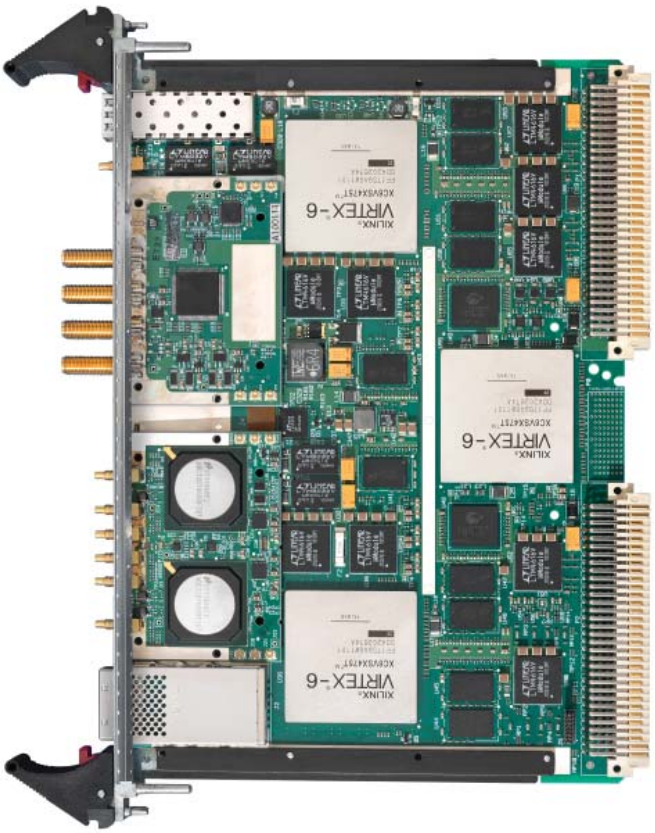
Two sample clock inputs are provided on the front panel, one for the ADC inputs and one for the DAC output. The input clock frequency for the ADCs is one-half the sample rate in the interleaved mode and equal to the sample rate in non-interleaved mode, resulting in a maximum ADC input clock frequency of 1.8 GHz in all modes. The ADC clock input has a minimum level of 0 dBm (nominal) while the DAC clock input has a minimum level of 6 dBm, both into 50 Ω.

Memory

The Gemini-V6 has two independent banks of onboard DDR3 SDRAM for each FPGA. The front end FPGAs have two 1 GB banks, each with throughput of 6.4 GB/s, while the back end FPGA has two 512 MB banks, each with throughput of 3.2 GB/s. The total memory capacity is 5 GB with aggregate throughput of 32 GB/s across six banks. All DDR3 memory banks are clocked at 400 MHz for an 800 MT/s transfer rate. In addition, there are two fully independent banks of QDRII+ SRAM memory for the back end FPGA. Each QDRII+ device has a 72 Mbit capacity (144 Mbit total) supported by an 18-bit data bus per bank.

System Monitoring

The Gemini-V6 includes facilities to monitor current and temperature at various points on the board. Current monitoring of all main power rails is available through the use of a Spartan6 FPGA. Die temperature monitoring of the three FPGAs and temperature monitoring of three locations on the PCB is also available. This allows a first level of protection when the Gemini-V6 is operating in different environmental scenarios. The output from the sensors is available to users' FPGA firmware applications, to allow the user application to adapt to changes in environmental conditions. The Gemini-V6 also uses the system monitoring sensors to implement a system protection mechanism which will, independently of the users' application, prevent excessive current or temperature from damaging the board.



PERFORMANCE SPECIFICATIONS

A/D Converter

Quantity: 1 or 3 channels
Sampling Rate: up to 1.8 GSPS (3 channel mode)
3.6 GSPS (1 channel mode)
Resolution: 12-bits
Type: ADC12D1800RF from National Semiconductor
Bandwidth: Up to 2.7 GHz

D/A Converter

Quantity: 1 channel
Sampling Rate: up to 4.0 GSPS
Resolution: 12-bits
Type: Euvis M653D
Bandwidth: Up to 4.0 GHz

Front Panel Analog Signal Inputs

Quantity: 3 ADC SSMC Connectors
Type: Single ended, AC coupled into 50 Ω, 3.2 dBm full scale

Front Panel Analog Signal Output

Quantity: 2 DAC SMA Connectors
Type: Single ended (differential as a build option), -4 dBm full scale

Front Panel Trigger Inputs

Quantity: 2 via 4 SSMC Connectors
Type: 100 Ω differentially terminated, support for LVDS and LVPECL (build option).
Mode: Independent or common for ADC and DAC modules

External Clock

Quantity: 2 SSMC Connectors
Type: Single ended 50Ω terminated
Input Power Range (ADC): 0 dBm (min) to 13 dBm (max)
Input Power Range (DAC): 6 dBm (min) to 10 dBm (max)
Operating Modes: Independent or common between ADC and DAC modules

Memory

DDR3 SDRAM (2 fully independent banks per FPGA)
Size: 1 GB per front end bank, 512 MB per back end bank
Bus Width: 64-bits per front end bank, 32-bits per back end bank
Speed: 400 MHz clock rate, 800 MT/s

QDR II+ SRAM (2 fully independent banks for back end FPGA)
Size: 72 Mbits per bank (144 Mbits total)
Bus Width: 18-bits per bank
Speed: Up to 500 MHz clock rate

Backplane I/O

VME Interface: A32:D32 slave interface
VXS Interface: P0 connector supports 8X high speed serial links
GPIO Interface: P2 connector
RACE++ Interface (Optional): P2 Connector can be configured to support RACE++ environments
Rear Transition Module (Optional): For rear access to the board, a Rear Transition Module is available which provides connections for GPIO connections, network access, PPS, and trigger signals

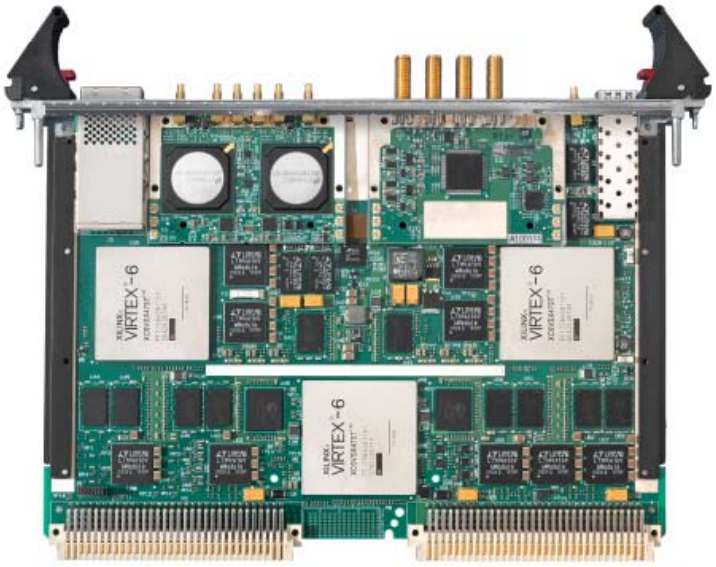
Size

Standard ANSI/VITA 1.1-1997 (R2003) VMEbus board, 6U x 4HP, single 0.8” slot
Optional VXS P0 connector for backplane I/O

Power

+5V, +3.3V, ±12V from backplane. Power consumption is dependent on customer application. Power estimation model is provided as part of the Developers Kit.

Contact factory for additional performance details.



Environmental / Ruggedization

In addition to providing high performance, Tekmicro boards and systems have been designed for ruggedization and power management. Tekmicro products operate effectively in laboratory, rugged air-cooled and rugged conduction-cooled environments to meet the needs of deployed applications.

Ruggedization Options

Specification	Commercial	Rugged Level 2	Rugged Level 3
Cooling	Convection	Convection	Conduction
Operational Temperature	0 to +55 °C (300 LFM airflow)	-40 to +70 °C (600 LFM airflow)	-40 to +85 °C (At Card Edge)
Storage Temperature	-40 to +85 °C	-55 to +100 °C	-55 to +125 °C
Relative Humidity	10% to 95% non-condensing	5% to 95% non-condensing	0% to 95% non-condensing
Conformal Coating	No	Yes	Yes
Shock	½ sine pulse, 20 g, 11 ms	½ sine pulse, 20 g, 11 ms	½ sine pulse, 40 g, 11 ms
Vibration (Sine)	2 g peak 15 to 2,000 Hz	10 g peak 15 to 2,000 Hz	10 g peak 15 to 2,000 Hz
Vibration (Random)	0.003 g^2/Hz from 15 to 2,000 Hz	0.04 g^2/Hz from 15 to 2,000 Hz	0.1 g^2/Hz from 15 to 2,000 Hz

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Tekmicro

TEK Microsystems, Inc.
300 Apollo Drive
Chelmsford, MA 01824
voice: +1.978.244.9200
fax: +1.978.328.5951
email: sales@tekmicro.com
web: www.tekmicro.com