Tekmicro

The Leader In FPGA-based Sensor I/O Processing

JazzFiber-V5 Serial FPDP I/O Module

- Two or Four Fiber Optic Interfaces (Up to 25.6 Gb/s Aggregate Throughput)
- ANSI/VITA 17.1-2003 & 17.2 Serial FPDP Support
- Fully Ruggedized – Including Conduction Cooled
- Supports Both PCI -X 64/133 & PCI Express x8

Features	Benefits
Standard LC Fiber Optic Transceivers	Compatible with both single and multi mode applications across a range of speeds
Latest Xilinx Virtex-5 FPGA Technology	Supports ANSI/VITA 17.1 Serial FPDP today with updates for 17.2 as the standard evolves
512 MB of DDR3 Memory	Provides deep memory buffers to easily support high throughput streaming I/O at full data rate
PCI-X 64/133 & PCI Express x1, x2, x4 & x8	Supports migration from PMC to XMC in a single module with a common driver without compromising performance

Overview

The JazzFiber-V5™ Serial FPDP I/O Module provides a high speed connection between one or more external sensors and a processing or recording system using an open standard modular I/O architecture. Each JazzFiber-V5 module supports four fiber optic interfaces, which can be used as separate Serial FPDP channels or aggregated into logical streams using the channel bonding capability of the emerging VITA 17.2 standard. Additional VITA 17.2 features including enhanced protocol and higher bit rates are also supported.

The JazzFiber-V5 is carefully designed to maximize performance in hardware, firmware, and software to support wire speed throughput between external sensor(s) and the user's baseboard. Each element of the module's design – fiber optic transceivers, FPGA, memory, and local bus/fabric interfaces – is optimized for maximum throughput to meet both current and future Serial FPDP requirements. The hardware is supported with optimized firmware and software drivers for a range of operating environments, making the JazzFiber-V5 easy to drop in and get running quickly.

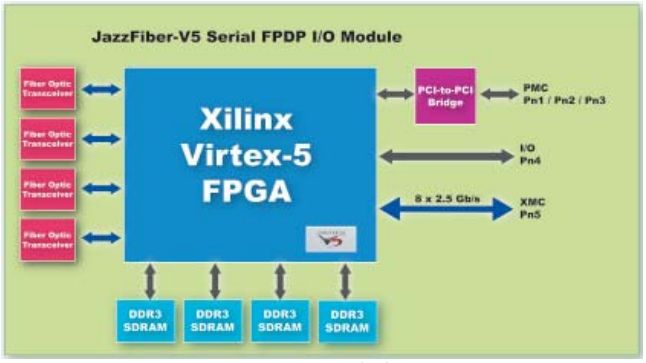


Figure 1: FPGA IP Block Diagram

Front Panel I/O

The JazzFiber-V5 can be configured with two or four LC-style fiber optic transceivers mounted at the front panel of the module. The fiber optic transceivers may be ordered with either single or multi-mode fiber interfaces at either 850 or 1310 nm wavelengths. The baseline module supports baud rates of 2.5 Gb/s, with alternate speeds between 1.062 and 6.25 Gb/s.

The JazzFiber-V5 provides a separate discrete LVTTL or EIA-422 interface via front panel SSMC connectors which may be used for trigger or time base functions.

Wavelength	Cable	Baud Rate	Max Distance
850 nm	50 / 62.5 µm multimode	2.5 Gb/s	150 m
1300 nm	9 µm single mode	2.5 Gb/s	2 km

Table 1: Fiber Optic Interface Options

Serial FPDP Protocol

The JazzFiber-V5 implements the Serial Front Panel Data Port (FPDP) protocol, an open standard for sensor-to-processor data links defined by ANSI/VITA 17.1-2003. Serial FPDP provides low protocol overhead, support for synchronization primitives in the data stream and high efficiency.

Serial FPDP supports baud rates of 1.062, 2.125, and 2.5 Gb/s, with net data rates up to 247 MB/s after data encoding and protocol overhead. Serial FPDP has been deployed in a wide range of sensor I/O applications and is a well established tool for moving large amounts of data between external sensors and signal or data processor systems.

The latest generation of Serial FPDP is being finalized as VITA 17.2. It adds several enhancements to the protocol, including official support for higher baud rates, channel bonding, and protocol enhancements. VITA 17.2 serial FPDP protocol extensions support baud rates up to 6.25 Gb/s. The JazzFiber-V5 supports many of the elements of 17.2. Tekmicro will continue to update firmware as the standard is finalized.

# of Fibers	Baud Rate	Aggregate Throughput
One	1.062 Gb/s	105 MB/s
One	2.5 Gb/s	247 MB/s
One	6.4 Gb/s	633 MB/s
Four	2.5 Gb/s	997 MB/s
Four	6.4 Gb/s	2553 MB/s

Table 2: Serial FPDP Throughput

Virtex 5 FPGA

The JazzFiber-V5 uses a Xilinx Virtex-5 FPGA to implement the interface protocol, memory buffering, DMA engines, and local bus/fabric interface. The installed FPGA device depends on the number of channels and the serial baud rate, ranging from a two channel 2.5 Gb/s module which uses an LX50T, to a four channel 6.25 Gb/s module using an FX100T.

The FPGA bitstream is automatically loaded from onboard FLASH memory at power up. Utilities are provided to program and verify FLASH memory to support bitstream updates in the field.

DDR3 Memory Buffers

The JazzFiber-V5 uses the latest memory technology – DDR3 – to provide maximum memory throughput at 23% less power than DDR2 based memory. With four independent memory banks clocked at 400 MHz each, the buffer memory subsystem provides aggregate throughput of 6.4 GB/s, supporting full rate deep FIFO buffering of the maximum 25 Gb/s fiber optic capability.

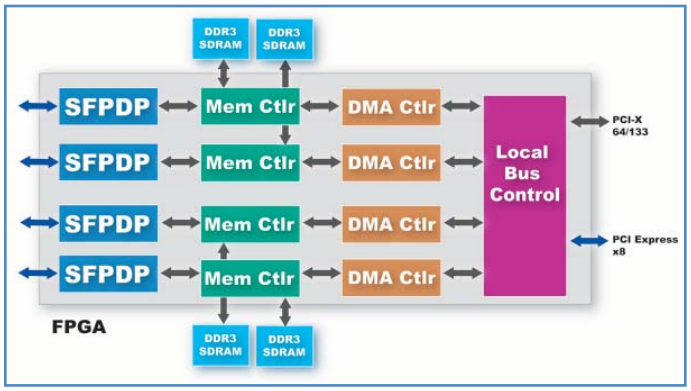
The baseline module has 512 MB of memory, which provides up to 500 ms of buffering at full 17.1 Serial FPDP rates, decoupling the module from local bus memory latencies.

Technology	Speed	Power (per 1 GB/s)
DDR (JazzFiber)	133 MHz (2.1 GB/s)	2200mW
DDR2	333 MHz (5.3 GB/s)	290 mW
DDR3 (JazzFiber-V5)	400 MHz (6.4 GB/s)	190 mW

Table 3: Comparison Serial FPDP Memory Buffer Technologies

Local Interface

The JazzFiber-V5 provides two high performance local interfaces: PCI and PCI Express. The PCI interface operates at up to 64-bit 133 MHz (PCI-X) and is compatible with the IEEE 1386.1-2001 PCI Mezzanine Card (PMC) standard as well as ANSI/VITA 39-2003.



To provide maximum compatibility with legacy systems, an onboard PCI-to-PCI bridge is used to support legacy PCI carriers from 32-bit 33 MHz up to 64-bit 133 MHz with universal I/O signal level compatibility. When connected to a high performance carrier with a 64-bit 133 MHz bus, the PCI interface sustains performance of up to 900 MB/s.

The JazzFiber-V5 supports a local fabric interface using the PCI Express protocol. The PCI Express interface is compatible with the VITA 42.0 Switched Mezzanine Card (XMC) base standard along with its PCI Express variant, ANSI/VITA 42.3-2006. The PCI Express interface implements x1, x4, or x8 serial lanes at 2.5 Gbps each with throughput up to 2.0 GB/s in each direction.

Standard	Architecture	Mode	Max Throughput
PCI	Bus	32 bit 33 MHz	133 MB/s
PCI-X	Bus	64 bit 66 MHz	533 MB/s
PCI-X	Bus	64 bit 133 MHz	1067 MB/s
PCI Express	Fabric	1 x 2.5 Gb/s	2 x 250 MB/s
PCI Express	Fabric	4 x 2.5 Gb/s	2 x 1000 MB/s
PCI Express	Fabric	8 x 2.5 Gb/s	2 x 2000 MB/s

Table 4: Local Bus / Fabric Throughput

System Management

The JazzFiber-V5 includes system monitoring functions that monitor load current and operating temperature at key points on the card. In the event of a fault condition, an alert is raised to the host for appropriate action. The system monitoring is also available through the XMC I2C interface for environments that implement IPMI capability.

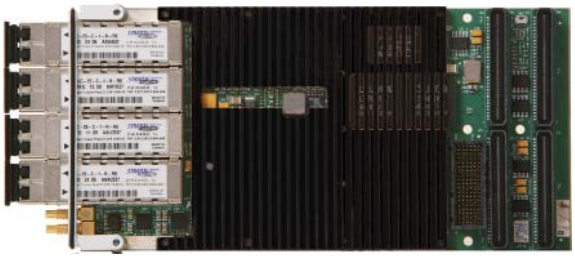
Software Support

The JazzFiber-V5 includes driver support for Windows, Linux and VxWorks, allowing the module to be used in a wide range of target environments. The software application programming interface (API) is common across all three operating environments, providing a reusable solution across both x86 and PowerPC platforms in many different form factors. Please consult with the factory about host support for specific carriers, processors and operating environments.

The software drivers are tightly coupled to the onboard DMA controllers implemented in the Virtex-5 FPGA, providing independent control of each Serial FPDP transmit and receive stream. The DMA engines support all of the Serial FPDP framing modes (unframed, fixed length and variable length), allowing the user application to easily support any type of Serial FPDP sensor. Aggregation of 17.2-compliant channel bonded streams is handled transparently by the firmware, providing the software with a single “stream” interface to both single and multiple physical fiber streams.

Customization

Tekmicro offers a customizable FPGA-based processing platform for applications that require additional flexibility. It is available with an expanded range of FPGA devices (LX110T, LX155T, SX95T and FX100T) and can be used to implement alternate external I/O protocols as well as alternate local fabric interfaces such as Serial RapidIO (ANSI/VITA 42.2) and Xilinx Aurora (VITA 42.5). Please consult the factory for additional information.



PERFORMANCE SPECIFICATIONS

Fiber Optic I/O
Serial Baud Rate: 2.5 Gb/s standard, 1.062 to 6.4 Gb/s options available
Interface: 850 nm for 50 / 62.5 µm multimode fiber standard, other options available

Serial FPDP
Compliant to ANSI/VITA 17.1-2003, VITA 17.2 (draft 0.6)
Supports framing modes (unframed, fixed size, dynamic size)
Supports flow control
Supports copy and copy/loop modes
Supports sync with and without data valid

PCI Local Bus
Compliant to IEEE 1386.1-2000 PCI Mezzanine Card (PMC)
Compliant to ANSI/VITA 39-2003
Compliant to PCI 2.3, PCI-X 1.0, up to 64-bits, 133 MHz
Supports 3.3V and 5V I/O signaling

PCI Express
Compliant to VITA 42.0 and ANSI/VITA 42.3-2006
Compliant to PCI Express 1.0a
Supports x1, x2, x4, x8 at 2.5 Gb/s per link

Mechanical
(L) 149mm (5.66”) x (W) 74mm (2.91”)

Power
Requires 5 Volts (PMC) or 5 to 12 Volt Vpwr (XMC), automatically selected
Typical Power: 15 Watts

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