High Resolution Range-Doppler Radar Demonstrator Based on a Commercially Available FPGA Card

Henning Nicolaisen[#1], Tor Holmboe[*2], Karina Vieira Hoel[*3], Stein Kristoffersen[*4]

[#]*University of Oslo, Department of Informatics*
P.O. Box 1080 Blindern, NO-0316 Oslo, Norway
[1]henning.nicolaisen@fys.uio.no

[*] *Norwegian Defence Research Establishment*
P.O. Box 25, NO-2027 Kjeller, Norway
[2]tor.holmboe@ffi.no
[3]karina-vieira.hoel@ffi.no
[4]stein.kristoffersen@ffi.no

***Abstract*— An X-band high resolution range-Doppler radar demonstrator has been developed, based on a commercially available 6U-VXS form-factor digital signal processing card containing all necessary base-band circuitry. The custom design covers a radio frequency up-down converter, FPGA firmware and PC software. The practical signal bandwidth is close to 1GHz and the range resolution is close to 15cm. The functionality has been demonstrated in a free space radiation experiment.**

I. INTRODUCTION

Where space or weight is limited, a single generalized hardware platform that can switch between a wide range of roles or functions merely through reconfiguring the software and firmware, is highly desirable.

Traditionally, radio frequency (RF) systems are based on dedicated hardware, such as ASIC-circuits. Such hardware offer little or no reconfigurability and the possibility of reusing the system for other applications is limited. The current development of generalized commercial-off-the-shelf (COTS) hardware modules is about to change this situation. Modules incorporating high speed and high bandwidth analog-to-digital converters (ADC) and digital-to-analog converters (DAC) along with ample digital signal processing resources, especially field programmable gate arrays (FPGA), ease the implementation of such multi-purpose systems. An FPGA can be reconfigured in a matter of seconds, enabling rapid switching between the different functions.

This paper describes the application of one such module, the TRITON VXS-1 [1] card, in a planned multi-purpose RF technology demonstrator called MuPuRF. The MuPuRF system is planned to demonstrate capabilities in radar and radar electronic warfare (EW), i.e. electronic attack (EA) and electronic support (ES). The first version of the radar mode has now been implemented and tested and is reported here. The other modes of MuPuRF remain to be implemented.

The radar resolution in range and Doppler can be varied within wide limits, from the resolution typical of air target range-Doppler radars to the high resolution representative of synthetic aperture radars (SAR) and inverse SAR (ISAR) systems. However, no radar trajectory compensation, antenna steering or target following function is implemented and the MuPuRF radar mode does not represent an operational system in this respect. The Nyquist digital signal bandwidth of MuPuRF is 1 GHz, corresponding to 15 cm theoretical range resolution.

Figure 1 MuPuRF radar system

Figure 1 shows the various hardware units of the MuPuRF system. The TRITON is mounted in a 5-slot VXS Crate. The only function of the back plane is to supply power. The RF up-down converter unit is shown in its preliminary form, assembled on the aluminium plate in the foreground. The receiver (Rx) low-noise amplifier (LNA), the transmitter (Tx) power amplifier (PA) and the cabling is not depicted.

II. TRITON VXS-1 CARD

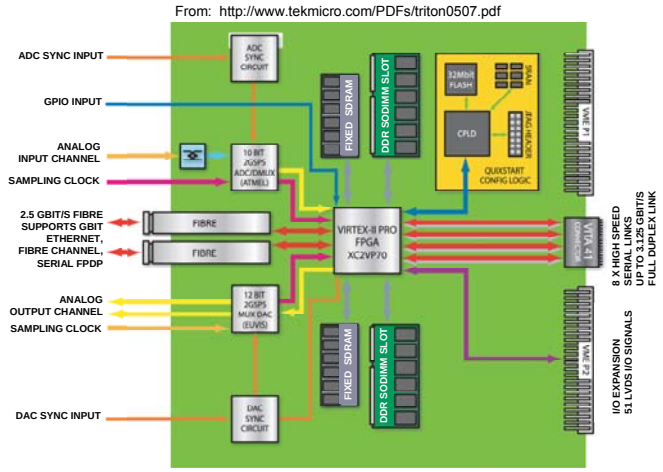

Figure 2 TRITON VXS-1 main components and signal paths

The TRITON VXS-1, produced by Tekmicro [2], is a single-slot 6U form factor card and is in accordance with the VITA 41.0 VXS specification. The advertised key applications for the TRITON VXS-1 include radar, electronic warfare, software radio and telecommunications. Figure 2 shows the main components and signal paths. The core of the TRITON VXS-1 is a Xilinx Virtex-II Pro FPGA circuit along with a 10bit ADC and a 12bit DAC. Both converters can operate at 2 GSamples/sec, giving a Nyquist digital signal bandwidth of 1 GHz. The analog 3 dB-bandwidth extends from 3 MHz to 3 GHz.

The VXS standard has inherited the connectors P1 and P2 from the VME 64 standard, but they are only used for powering the card. The VME bus interface itself is not implemented except for 51 user defined signals in connector P2. Control and high speed data IO for the card is preferably implemented using the high speed serial links available on the front panel (e.g. Gigabit Ethernet) and/or the backplane VXS P0 connector, located between P1 and P2.

The card contains two banks of 0.5 GByte fixed DDR SDRAM memory and two DDR SODIMM module sockets accepting up to 2 Gbyte modules each, giving a total maximum memory capacity of 5 GByte. The actual system at hand however has a total memory capacity of 2 GByte. The internal memory of the FPGA comes in addition.

The FPGA can be configured in three ways: from on-board flash memory during power up, via the on-board JTAG connector or via Gigabit Ethernet on the front panel.

A developers kit is available which contains libraries of FPGA intellectual property (IP) cores and PC software. The kit also contains FPGA and PC source code for two reference designs. The first is a combined snapshot data capture and arbitrary waveform generator system, and the second is a loop-around system running the ADC data directly to the DAC. Suitable design environment is Xilinx ISE and Microsoft Visual Studio.

III. MUPURF RADAR DESIGN AND FUNCTIONALITY

Figure 3 shows a functional block diagram of the MuPuRF radar system. It consists of three main units, the RF up-down converter, the TRITON and a laptop computer running the graphical user interface (GUI). An Rx LNA and a Tx PA is also depicted. The radar uses separate Rx and Tx antennas, and is capable of simultaneous Rx and Tx operation.

Single channel single stage RF up-down conversion is employed. A more complex up-down converter may be needed in order to enable multi-purpose operation, but the present design is adequate for limited X-band lab-radar operation. The sensitivity at the RF-input connector is such that a -45 dBm input level corresponds to the full scale range of the 10 bit ADC. Any LNA gain comes in addition. A high-speed programmable, 60 dB range, attenuator can be utilized to compensate for the $1/R^4$ range dependency and to perform general sensitivity adjustments under software control.

The FPGA is mainly utilized for the time critical functions involved in transmitting the Tx pulse waveform to the DAC at a steady pulse repetition frequency (PRF), and to record the corresponding echoes from the correct range interval or scene. These control functions are implemented in the main state machine. Set-up parameters such as pulse length, start and stop of the scene, pulse repetition interval (PRI) and the number of pulses in the Doppler processing interval are selected in the PC GUI and transferred to the TRITON. Up to four different PRIs can be programmed for automatic consecutive pulse bursts in order to resolve range or Doppler ambiguities.

The radar can operate using any kind of waveform within the maximum 1 GHz bandwidth. The desired waveform is selected and generated in the PC GUI and transferred to the TRITON together with the rest of the radar parameters. The pulse length is presently limited by the Tx-FIFO memory size of 8 kSamples in the current configuration. With a full bandwidth waveform (i.e. 2 G Samples/s) this is equivalent to a 4 µs pulse.

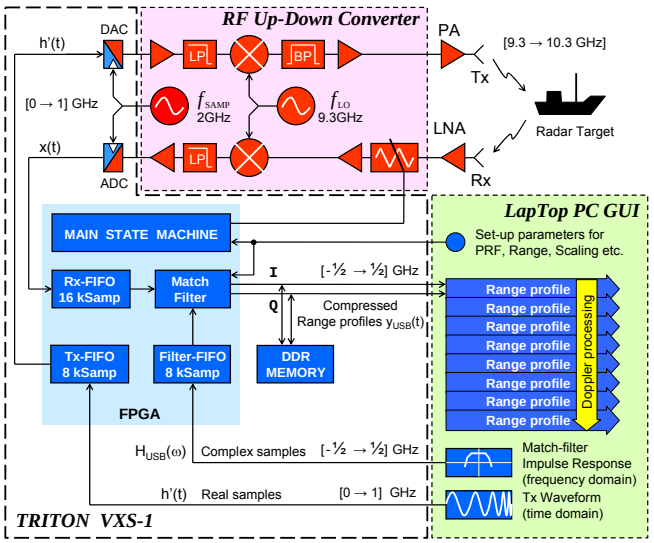

Figure 3 MuPuRF radar system functional block diagram

The digitized base-band Rx signal is buffered in the Rx-FIFO memory upon reception. The size of this buffer is 16 kSamples corresponding to a sampled maximum range interval of 1229 m in the case of a full 1 GHz bandwidth waveform.

In case the waveform has a fraction 1/N of the full bandwidth the effective sampling speed could be reduced accordingly through resampling the DAC and ADC data streams internally in the FPGA. This would effectively increase the maximum pulse length, the range cell size and the maximum scene length by the factor N, while maintaining the processing speed.

A combined real-time match filter and quadrature demodulator is implemented in the FPGA. The required filter response is transfered from the PC to the FPGA filter-FIFO. The implementation of the combined filter-demodulator is described in chapter IV. The processing delay of the filter-demodulator depends on the number of Rx samples, and is the limiting factor of the maximum PRF obtainable in real-time operation. In case of higher PRFs, the FPGA filter-demodulator must be omitted, and the function performed at much lower speed in the PC in stead. The output of the FPGA filter-demodulator, i.e. the compressed range profiles, is buffered to the TRITON DDR RAM and subsequently transfered to the PC for Doppler processing, display and data storage.

All data transfer, configuration and control signals between the TRITON and the PC run via Gigabit Ethernet.

The FPGA design is developed in the Xilinx ISE environment, utilizing the TRITON developers kit IP cores for interfacing to the ADC, DAC, DDR RAM and Gigabit Ethernet.

The GUI with its underlying processing and functions is developed under Visual Studio, and runs on the laptop computer with a Windows XP operating system.

IV. Match Filter and Quadrature Demodulator

The Tx base-band signal denoted h'(t) is selected and generated in the PC GUI as a 2 GS/s time-series consisting of real samples. The time domain impulse response h(t) of the optimal linear match filter is equal to a time-reversed version of the transmitted pulse h'(t) [3]. The output y(t) of such a linear match filter is the convolution of the impulse response h(t) with the received echo x(t). Furthermore its Fourier spectrum Y(ω) is equal to the complex product of the spectra H(ω) and X(ω) [3]. In MuPuRF this latter relationship is utilized as the match filtering is performed in the frequency domain through employing the Fast Fourier Transform (FFT) and the inverse FFT (IFFT) as shown in Figure 4. The time-series h(t) is zero-extended in order for H(ω) to have the same resolution as X(ω).

Furthermore, the output of the match filter y(t), i.e. the compressed range profile, needs to be quadrature demodulated into in-phase and quadrature components I&Q in order for the subsequent Doppler processing to be able to distinguish between positive and negative Doppler shifts. As the transmitted signal consists of real samples only, so will the compressed echo y(t). The Fourier spectrum of y(t) is therefore symmetric around zero, consisting of an upper (USB) and a lower (LSB) sideband with identical content, as depicted in the upper panel of Figure 5. The quadrature demodulation is performed in the frequency domain through down-shifting the USB of the spectrum by the amount ½Nyquist frequency, and at the same time discarding the lower side band (LSB). This process is depicted as the transition from $Y(\omega)$ to $Y_{USB}(\omega)$ in Figure 5. Since $Y_{USB}(\omega)$ is not symmetrical around 0 Hz, the corresponding time-series $y_{USB}(t)$ is complex, i.e. consists of I&Q components. The number of discrete samples in $Y_{USB}(\omega)$ is half as many as in $Y(\omega)$ and the number of samples in $y_{USB}(t)$ is half as many as in y(t). The sample rate of $y_{USB}(t)$ is thus 1 GHz. For computational reasons, the quadrature demodulation has been pushed back and is employed on the match filter transfer function $H(\omega)$ and the received echo $X(\omega)$ rather than directly on $Y(\omega)$, as depicted in Figure 6.

The implemented FFT and IFFT is a Xilinx Coregen IP, the FFT v5.0 [4], having a radix-4 architecture and unscaled, fixed point, arithmetic. The FFT has the input width set to (10+10) bit and the output is (25+25) bit. The input from the

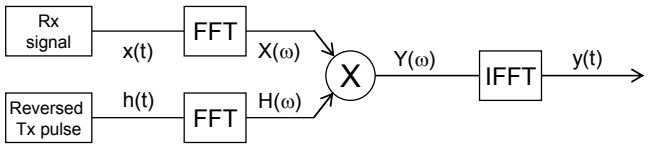

Figure 4 Match filtering in the frequency domain

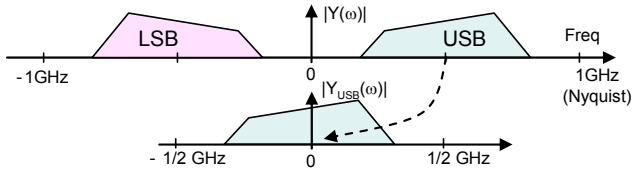

Figure 5 Quadrature demodulation

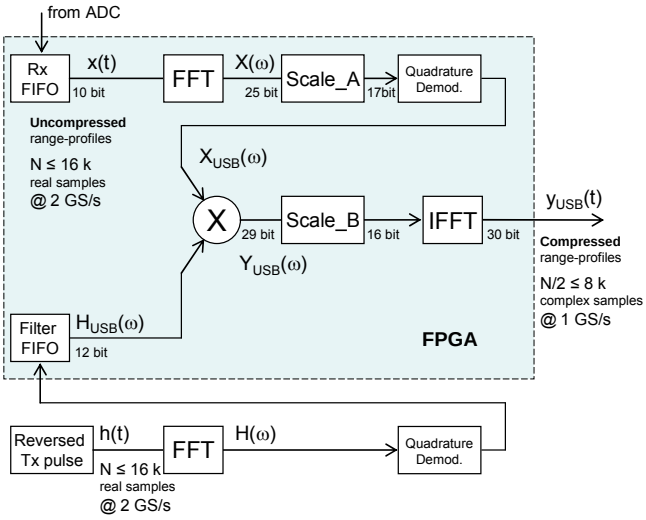

Figure 6 Combined match filter and quadrature demodulator

ADC is real and the imaginary input component is therefore set to zero. The IFFT has the input width set to (16+16) bit and the output is (30+30) bit.

The components Scale_A and Scale_B, shown in Figure 6, are semi-constant scalers. The scalers are programmed by the PC GUI based on the anticipated or observed signal intensity. An alternative approach would have been to use scaled or floating point FFT in stead. Such components however use higher bit-widths demanding more FPGA resources, and are therefore only feasible in the FPGA at hand with a substantially reduced filter length.

V. Simulation of the Combined Match Filter and Quadrature Demodulator

Figure 7 shows a MatLab simulation of the combined match filter and quadrature demodulator as described in Chapter IV, but with all signals and processes being floating point.

All horizontal axes are index numbers rather than absolute values in meter or Hertz. The left column shows time-series. The right column shows the corresponding Fourier spectra with 0 Hz in the centre, i.e. the right hand side of the spectra represents the USB.

Panel A and B shows the pulse code; a linear up-chirp, 256 samples long, centered at ½Nyquist and with a frequency bandwidth equal to ½Nyquist.

Panel D shows the impulse response of the match filter, which includes a Hanning data window to suppress the pulse compression sidelobes typical for a chirp-type signal. The response has been zero-padded up to the length of the sampled echo, which is 1024 in this simulation.

Panel F shows the echo from three, equal intensity, scattering points located at the ranges 100, 300 and 600 respectively and with Doppler frequencies 30, -50 and 40 respectively. The Doppler frequencies correspond to Doppler processing based on 128 pulses, i.e. the processed Doppler spectrum has 128 cells indexed from -64 to +63. The Doppler

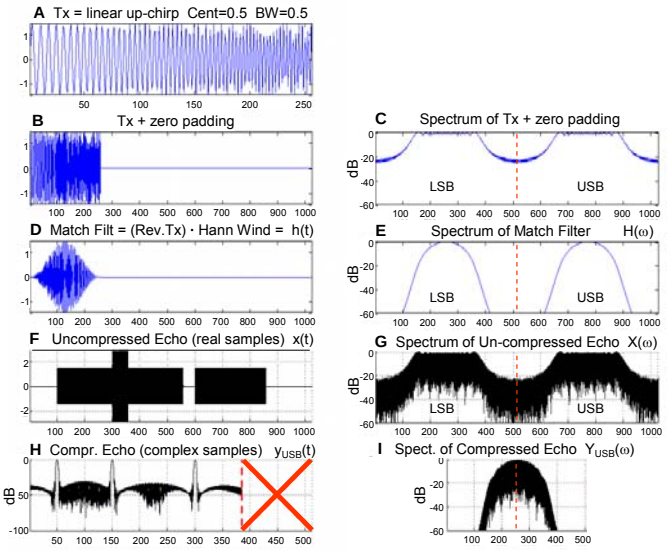

Figure 7 Matlab simulation of match filter and quadrature demodulator

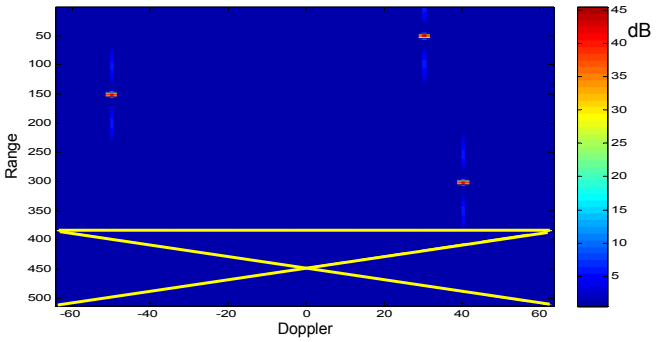

Figure 8 Range-Doppler image of the simulated data in Figure 7

frequencies are not evident in Figure 7, but do show up in the range-Doppler image in Figure 8.

Figure 7, panels F through I show all the 128 pulses superimposed. Figure 7-H shows the compressed range profiles, hence the halved range index due to the quadrature demodulation. The compressed range profiles have been left-shifted by an amount equal to the latency of the filter, i.e. the length of the transmitted pulse. This leaves a gap of corresponding size at the trailing end, marked by a red cross.

Figure 8 shows the range-Doppler image that results from Doppler processing the 128 compressed range profiles in Figure 7-H. The Doppler processing employs a Hanning data window, in order to reduce any Doppler sidelobes induced by spectral leakage. The range area marked by the yellow cross correspond to the red cross in Figure 7-H.

VI. FPGA Resource Utilization & Performance

Referring to Figure 6, the complex product $X_{USB}(\omega)\cdot H_{USB}(\omega)$ and the complex products within the FFT and IFFT utilize the 18 bit by 18 bit hardware multipliers, the MULT18x18, available in the Xilinx Virtex II architecture.

The three FIFO-memories implemented in the FPGA are based on the Block-RAM (BRAM) hardware component. In addition the FFT core uses a substantial amount of BRAM to hold the data during calculation.

A summary of the required FPGA resources for the MuPuRF system is presented in Table I. The second column shows the available resources. The next columns show the resource requirements for three different cases; without any match filter implemented, with a 16 kSamples match filter and with a 32 kSamples match filter. As can be seen, the number of available BRAM cells in the Virtex-II Pro circuit limits the maximum length of the match filter to 16k samples.

TABLE I
FPGA Resource Requirement

	FPGA Resource Utilization						
	Available	**MuPuRF No Filter**		**MuPuRF 16k filter**		**MuPuRF 32k filter**	
Slices	66176	12121	18%	23049	34%	23472	35%
4-input LUT	66176	10192	15%	21523	32%	22845	34%
IOB	964	662	68%	662	68%	662	68%
BRAM	328	102	31%	288	87%	**411**	**125%**
MULT 18 x 18	328	0	0%	60	18%	60	18%

TABLE II
MATCH FILTER TIMING

			Non-pipelined		Pipelined	
Echo length (samples)	**Data collection time @ 2 GS/s (us)**	**Sampled Range @ 2 GS/s (m)**	**Total time (us)**	**Maximum PRF (kHz)**	**Total time (us)**	**Maximum PRF (kHz)**
128	0.06	9.6	4.2	238.1	2.5	396.8
256	0.1	19.2	8.4	119.0	5.0	198.4
512	0.3	38.4	16.8	59.5	10.1	99.2
1024	0.5	76.8	33.0	30.3	19.8	50.5
2048	1.0	153.6	67.0	14.9	40.2	24.9
4096	2.0	307.2	134.0	7.5	80.4	12.4
8192	4.0	614.4	268.0	3.7	160.8	6.2
16384	8.0	1228.8	536.0	1.9	321.6	3.1

The processing delay of the match filter limits the maximum PRF of the system. Table II shows the relationship between the length of the echo to be processed and the maximum PRF. The timing for both a non-pipelined and a pipelined operation of the match filter is shown. In the pipelined mode the FFT-cores allow new data to be shifted in at the same time as the result data are shifted out. Performing these operations simultaneously increases the performance of the filter with approximately 40% compared to the non-pipelined mode. The data collection time in column #2 represent scenes starting at zero range. If the scene is to start further downrange, 1μs per 150m must be added to the total time, reducing the maximum PRF accordingly.

VII. SUMMARY OF SPECIFICATIONS

A summary of the specifications for the MuPuRF radar system is shown in Table III. Numbers for the low-noise amplifier, power amplifier and antenna gains are not included.

TABLE III
SPECIFICATIONS SUMMARY

Center Frequency	9.8 GHz (X-band)
Nyquist Bandwidth	1 GHz
Minimum Range	0
Maximum Range	38400 m *
Maximum Scene Length	Up to 16 kSamples **
Maximum PRF	see Table II
Maximum PRI	16 ms
Maximum Pulse Width	8 kSamples (i.e. 4 μs @ 2GS/s)
Minimum Pulse Width	2 Samples (i.e. 1 ns @ 2 GS/s)
Maximum Number of Pulses	62500 ***
Sensitivity at RF-input connector	-45 dBm #
Maximum level at RF-output connector	-4.5 dBm

* Max. number in range-counter only. Actual maximum range is in addition limited by Tx-power, antenna gains etc. The coherency at longer ranges also remains to be tested.
** Maximum scene length is the maximum number of range samples (i.e. 16 k) minus the number of samples in the pulse.
*** Capacity of 2 GByte DDR RAM with 16 kSamples per pulse
\# Corresponds to full-scale range at ADC

VIII. FREE SPACE RADIATION RESULTS

The MuPuRF radar mode has been tested in a free space radiation experiment. The experiment employed two versions of the match filter for comparison. The FPGA-implemented match filter was found to produce practically identical results as a software implemented floating point match filter in the PC.

A car was acting as radar target, circulating in the area in front of the radar at approximately 50 m distance to the antennas. The antennas were placed 3 m apart. The geometry is shown in the upper part of Figure 9. The car carried a small corner retroreflector mounted at the roof near the rear end. The antennas were at approximately 4 m elevation with respect to the car ground level, looking slightly downwards. Both antennas were horizontally polarized horn antennas with approximately 25º 3 dB main lobe. Maximum power at the Tx-antenna connector was on the order of 20 mW. Due to the short range no LNA was employed. The other radar parameters were as shown in Table IV.

TABLE IV
RADAR PARAMETERS

Centre Frequency	9.8 GHz
# Range samples, uncompressed	8192
Pulse Width	6192 Samples / 3.096 μs
Scene, compressed	1000 Samples / 0-150 m
Pulse Bandwidth	900 MHz
Pulse Code	Linear up-chirp
Amplitude Window, Range	Hanning
Pulse Repetition Frequency	500 Hz
# Pulses in Coherent Burst	128
Doppler Integration Interval	128/500 s = 0.256 s
Amplitude Window, Doppler	Hanning

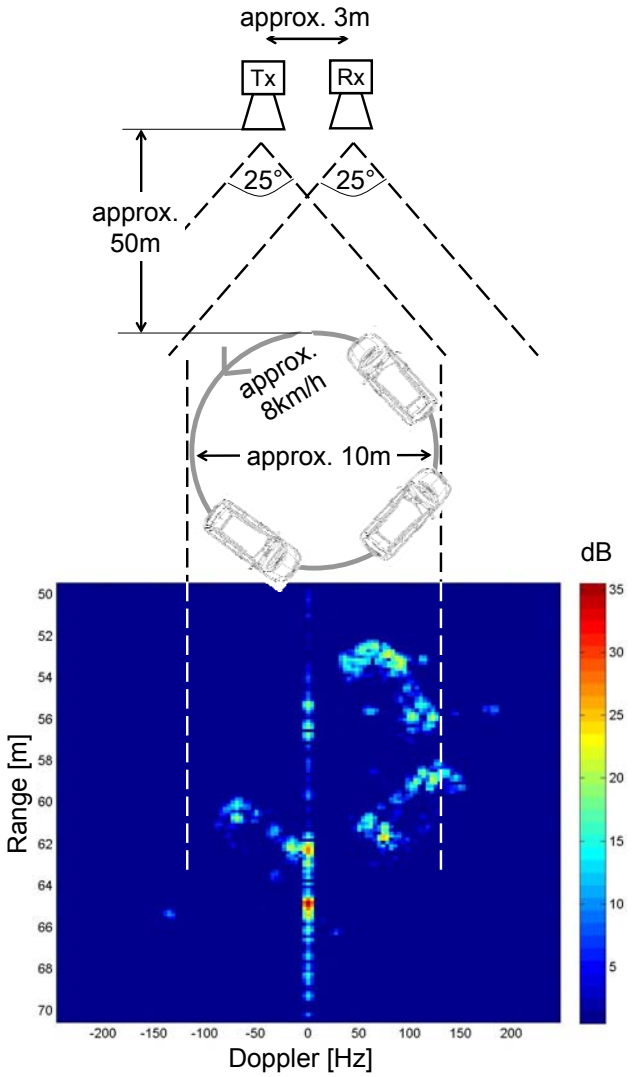

Figure 9 Geometry and radar results

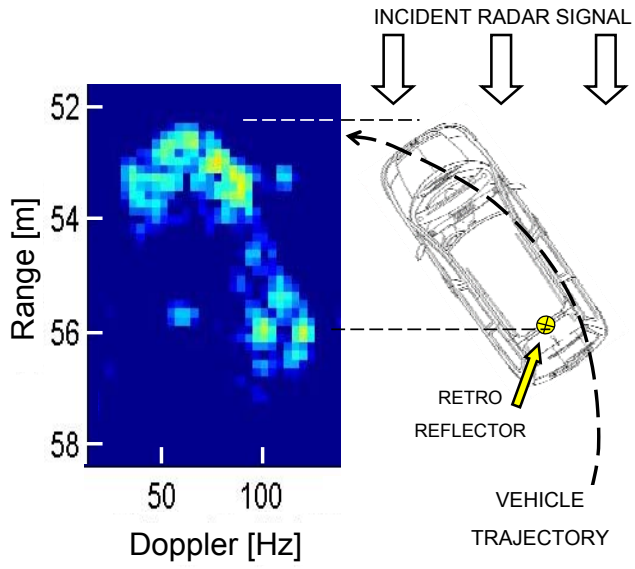

Figure 10 Geometry and radar results detailed plot

The range-Doppler image in Figure 9 is an overlay of three different images, with the car in three different positions as indicated in the geometry sketch. Each of these three images is based on 128 pulses, spanning 0.256 s. The zero-Doppler line is the result of buildings and parked cars within the processed scene as well as the ground itself. Figure 9 is zoomed in range, showing about 20 m of the 150 m long processed scene.

Figure 10 is even further zoomed in both range and Doppler and corresponds to the upper of the three images in Figure 9.

It should be noted that the images are pure range-Doppler images without any ISAR processing. The short Doppler processing interval with respect to the relatively low speed of the vehicle of approximately 8 km/h produces very little smearing of the images though. The features of the car can easily be recognized, and so can the corner retroreflector.

IX. Summary and Conclusion

The COTS card TRITON VXS-1 has proven to be a suitable hardware platform for performing the real-time base band functions required in the radar mode of the planned multi-purpose RF demonstrator. The radar has been tested in a free space radiation experiment with the combined match filter and quadrature demodulator implemented in FPGA, producing fully satisfying results for a 900 MHz bandwidth waveform. The theoretical range resolution for this bandwidth is 17 cm, which is in good accordance with the observed range resolution.

The TRITON is undoubtedly suited for the other planned functions and modes of the MuPuRF system, and the work of implementing these will proceed.

Acknowledgments

The authors wish to thank Steinar Johnsrud at FFI for assembling the RF up-down converter unit.

References

[1] (2008) Triton VXS-1 data sheet. [Online]. Available: www.tekmicro.com/PDFs/triton0507.pdf

[2] (2008) The Tekmicro website. [Online]. Available: www.tekmicro.com

[3] N. Levanon, *Radar Principles*, New York, USA: John Wiley & Sons, 1988.

[4] (2008) Xilinx Coregen Fast Fourier Transform v5.0 data sheet [Online]. Available: http://www.xilinx.com/ipcenter/catalog/logicore/docs/xfft.pdf