



QuiXilica V5 Architecture:

The High Performance Sensor I/O Processing Solution for the Latest Generation and Beyond

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Military sensor data processing applications for communications, radar, and electronic warfare have an insatiable demand for increased signal performance. Sensors continually require more channels, increased processing capabilities, higher memory performance and greater communications bandwidth.

Advanced applications in Radar, EW, ELINT, SIGINT and Telecom require the performance offered by the very latest component technologies of FPGAs, memories, communications standards, etc. To get the best out of these latest technologies, Tekmicro's new QuiXilica V5 Architecture encompasses a holistic architectural philosophy resulting in an advanced family of products that serves the needs of demanding sensor I/O applications.

The QuiXilica V5 Architecture builds upon the success of the current QuiXilica board family, utilizing Xilinx Virtex-5 FPGAs, DDR3 SDRAM and the latest enhancements in flexible I/O communication modules (SFP+ and QSFP). These components are carefully interconnected and balanced into an architecture optimized for target applications in sensor I/O processing.

QuiXilica V5 Architecture

The QuiXilica V5 Architecture is the basis for a variety of digitizer boards in multiple form factors. A very broad range of analog sensor I/O configurations provide easy compatibility with the widest range of analog signal options, addressing multi-channel, high resolution sampled data requirements at 4 Gsps (Gigasamples per second) and beyond.

QuiXilica V5 boards are designed to retain the strong underlying principles and core feature set of the previous generation of QuiXilica digitizers such as high speed front panel I/O, high signal integrity, high bandwidth memory, and significant FPGA resources.

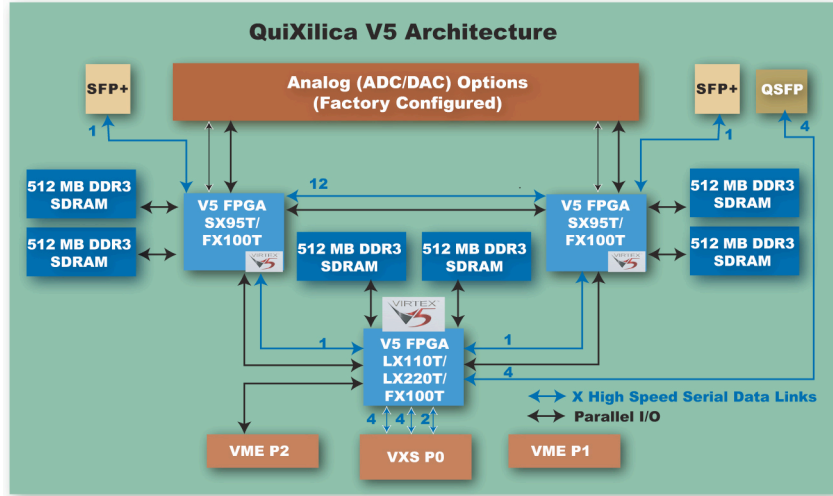


Figure 1 – VXS Payload Board using QuiXilica V5 Architecture

The first QuiXilica V5 digitizer boards, shown in Figure 1 above, will utilize the ANSI/VITA 41.0 VXS form factor. Future QuiXilica V5 products will extend the architecture into other form factors to give customers maximum choice and flexibility.

Latest In FPGA Processing

The Xilinx Virtex 5 FPGA family represents the high end of the “state of the art” in currently available FPGA processors. The initial members of the QuiXilica V5 Family use three Xilinx Virtex-5 FPGAs to provide maximum high bandwidth processing and system configuration flexibility. Each FPGA has access to two banks of DDR3 SDRAM of 512 MB each (1 GB total per FPGA). The QuiXilica V5 Architecture products will support 2 GB and 4 GB per FPGA when larger memory devices are available for increased storage density and increased memory bandwidth. Memory and FPGAs have been combined and interconnected using multiple high bandwidth parallel and high-speed serial interconnections; thus data can be available within the processing chain as needed, to meet a wide range of application requirements.

Inter-board and system communication requirements are met using either backplane connections or multiple front-panel high speed serial QSFP and SFP+ modules which provide eight and six high speed serial links respectively operating at up to 6.5 Gb/s. Utilizing the embedded communication functions as well as the QuiXilica core and software library support (QuiXtream), the QuiXilica V5 Family supports the latest generation of Open Standard I/O protocols such as Gigabit Ethernet, Serial FPDP (ANSI VITA 17.1 & 17.2), PCI Express, Xilinx Aurora and Fibre Channel.

In addition to providing high performance, QuiXilica V5 digitizers have also been designed for ruggedization and power management. QuiXilica V5 boards operate effectively in laboratory, rugged air-cooled, and rugged conduction-cooled environments to meet the needs of deployed applications.

TEK Microsystems provides superior QuiXilica FPGA cores and supporting firmware to minimize the effort required to extract maximum performance from the architecture, and to make development as easy as possible.

The Architecture’s common hardware interfaces and firmware /software development tools allow the user to easily migrate between platforms as different systems are developed, protecting the user’s investment both in their FPGA application and in integration and qualification of the QuiXilica V5 products in the target application.

Virtex 5 Processing

FPGAs are well established as the processor of choice for front-end-sensor applications, providing wide input data buses, large logic resources, substantial internal memory, high-speed serial transceivers and embedded DSP functions. The three Virtex-5 platforms providing embedded high-speed serial transceivers that can be utilized with the QuiXilica V5 products are the following:

- Virtex-5 LXT Platform - Optimized for high-performance logic with low-power serial connectivity
- Virtex-5 SXT Platform - Optimized for DSP and memory-intensive applications with low-power serial connectivity
- Virtex-5 FXT Platform - Optimized for embedded processing and memory-intensive applications with highest-speed serial connectivity

Virtex-5 FPGAs sharing the same footprint from any of the three platforms are pin-compatible. QuiXilica V5 digitizers can therefore be configured to use the most appropriate FPGAs from any of the three platforms to provide the most appropriate features and benefits for the particular application providing great flexibility.

Three key FPGA components (one from each family), shown in **Table 1**, have been identified as being the optimal balance of features / performance / cost for use on QuiXilica V5 digitizer boards:

	SXT95T	LX110T	FX100T
V5 Slices	14,720	17,280	16,000
18Kb BRAMs	488	296	456
Ethernet MACs	4	4	4
DSP48s	640	64	256
PCI Express Endpoints	1	1	3

Table 1 – Key FPGA component options for QuiXilica V5 digitizer boards

The SXT platform, with the greatest number of DSP48s, is well suited for implementing highly parallelizable algorithms such as wideband Digital Down Converters (DDCs), Finite Impulse Response (FIR) filters and Fast Fourier Transforms (FFTs). The SX95T is expected to be the FPGA of choice for two of the QuiXilicaV5 FPGAs which sit directly in the sensor data I/O paths.

The LX110T or FX100T are the preferred options for the third FPGA in the QuiXilica V5 Architecture sitting behind the two FPGA's mentioned above. This principally provides a control / communication resource alongside its raw data processing capability.

Alternate FPGAs may be considered for use in place of these standard devices with the QuiXilicaV5 digitizers pre-architected to support Virtex 5 parts up to LX330T or FX200T.

The FXT devices also provide embedded IBM440 PowerPC processors. The processors can be used for algorithmic functions or control applications as well as enabling the FPGA to support data recording and media management using the Tekmicro QuiXstore SoC core. By populating the board with three FXT devices, data recording solutions using up to six high speed Fibre Channel RAIDs can be implemented.

The default configurations, providing an optimal blend of features and power consumption for the QuiXilica V5 VXS digitizers are shown in **Table 2**.

	2 x SX95T + 1 x LX110T	2 x SX95T + 1 x FX100T	3 x FX100T
V5 Slices	46,720	31,040	48,000
18Kb BRAMs	1,272	1,432	1,368
Ethernet MACs	12	12	12
DSP48s	1344	1,536	768
PCI Express Endpoints	3	5	9

Table 2 – Default Configuration Options for QuiXilica V5 VXS Digitizer Boards

Configurable Analog Front-end

The QuiXilica V5 Architecture provides a simple flexible parallel interface that enables boards to be factory configured with different ADCs and DACs, thus enabling the boards to meet a robust variety of applications. High bandwidth support for ADCs and DACs operating beyond 4 Gsps is designed into the architecture.

Power supply quality is crucial to achieving expected performance from ADC and DAC front end components and the QuiXilica V5 Architecture has been very carefully designed to address the often neglected challenge of generating clean analog power sources in a noisy digital processing environment.

Building upon the success of the current QuiXilica board family and retaining a migration path for current users, the analog configuration options that are planned to be available for QuiXilicaV5 digitizers are:

- 6 x 16 bit 160MSPS ADC & 1 x DAC channel
- 7 x 16 bit 500 MHz DAC channels
- 2 x 10 bit 2.2 GHz ADC channels
- 2x 12 bit 2.2 GHz DAC channels
- 1x 10 bit 2.2 GHz ADC channels with 1x 12 bit 2.2 GHz DAC channels
- 6 x 12 bit 500MHz ADC channels
- 2 x 8 bit 4GHz ADCs channels
- + further configurations to be determined

Upon request and with limited engineering effort, further or alternative combinations of configurations can also be provided, enabling the architecture to support the latest mixed signal devices available now and in the future.

DDR3 SDRAM

Increased digitization data rates necessitate deeper and high bandwidth data buffers. To manage this need now and well into the future, QuiXilica V5 digitizers have been designed to utilize Double-Data-Rate-3 Synchronous Dynamic Random Access Memory (DDR3 SDRAM), the latest SDRAM technology commercially available.

The key features of DDR3 SDRAM are:

- Reduced power consumption - DDR3 uses 17% less power than DDR2
- Higher bandwidth - QuiXilica V5 banks are configured as 64 bits wide supporting a bandwidth of 6.4 GB/s
- Greater storage density

Firmware support for interfacing to the DDR3 memories facilitates easy integration of the DDR3 memory resources into user applications. FIFO style cores are provided which provide the user with a simple interface and high-throughput. Full random access cores are also available for more complex addressing schemes.

Backplane High Speed Serial Communications Resources

The QuiXilica V5 Architecture supports high bandwidth front-panel and backplane communications. Eight high-speed serial lanes are provided as per the VXS specification with achievable baud rates of up to 3.75 Gb/s per link (or 6.5 Gb/s if using FXT FPGAs). Using backplane links, multiple boards can easily be combined in standard backplanes to provide easily scalable systems capable of processing multiple sensor input channels.

Front Panel High Speed Serial Communication Resources

In some applications, it is also necessary to provide high speed connectivity through wired connections (e.g. using fiber optic cables). For example, it might be appropriate to interconnect discrete sub-systems (e.g. Sensor or processor boxes) based in separate, possibly remotely located areas. Alternatively, it may be necessary to include conventional server blade processors in a system, in which case wired connections are also required.

Recent developments in networking and high-speed serial communications have led to easy availability of commercial technologies for wired (fiber optic) interconnects which can support baud rates as high as 10 Gb/s. Two of these technologies (SFP+ and QSFP) have been implemented on the QuiXilica board family for wiring high speed serial connections into the front panel of the board.

SFP+ modules provide:

- Latest generation of Small Form-Factor Pluggable (SFP) modules
- Fully backwards compatible with SFP modules
- Support for baud rates up to 10 Gb/s
- Short or long wave fiber optic or 1000Base-T modules available
- 30% smaller size than 10 GbE XFP modules

For increased density, a Quad Small Form-Factor Pluggable (QSFP) module shown in **Figure 2** can also be used on the QuiXilica V5 digitizers. QSFP modules provide:

- Pluggable Copper & Optical Modules
- Four independent duplex lanes
- Support for baud rates up to 10 Gb/s
- Independent or bonded operation
- MPO style optical interface modules
- A range of fiber cables are available to provide break-out to LC connectors.

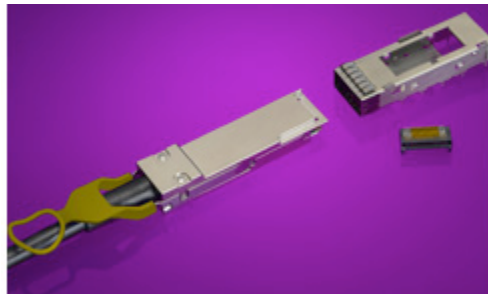


Figure 2 – QSFP module, cage and connector

Using the six high-speed serial lanes provided by the SFP+ and QSFP connectors, high bandwidth communications (limited only by the FPGAs) can be implemented for a range of applications. Up to six 4.25 Gb/s Fibre Channel links can be implemented to provide links to six RAIDs. Data processed on a QuiXilica V5 digitizer could be also distributed to six server blades for an alternative processing strategy.

Firmware and software support for a range of open standards and protocols is provided for the QuiXilica V5 family including Gigabit Ethernet, Serial FPD (ANSI VITA 17.1 and 17.2) and Fibre Channel. For inter-FPGA and inter-board communications, other protocol support is provided such as Xilinx Aurora and PCI Express.

System Health Monitoring

Due to the flexibility offered by FPGAs, it is conceivable that users could implement FPGA applications that, while valid, are problematic in terms of power and thermal management. The QuiXilica V5 Architecture includes a comprehensive System Health Monitoring facility to continuously track temperature and supply current at a number of key points in the system. If an impending fault condition is imminent, the system will automatically take action to remove the condition and it will alert the user to the problem as well as logging the occurrence.

Outputs from the system health monitoring sensors are available to user applications, if desired. This can provide useful diagnostic information during system development and testing or it can even be used dynamically within a deployed application, if required.

Power Estimation Tools and Ruggedization

FPGA based processing presents some tough challenges in terms of managing the power supply and heat dissipation from a hardware platform.

Generic statements of power supply requirements are effectively useless for FPGA based data processing architectures. Tekmicro provides software tools to allow users to analyze and experiment with the requirements of their design and the associated impact on power supply requirements. Supporting information and useful guides such as board power estimation tools and air flow resistance curves are available to assist the user in system and enclosure design. Using these tools, systems can be correctly specified and architected at a very early phase in the design process with a high degree of confidence.

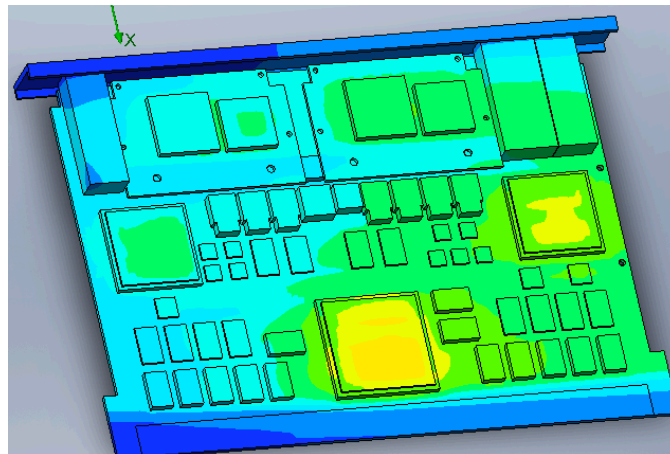


Figure 3 – Thermal modeling of QuiXilica V5 Digitizer

The QuiXilica V5 Architecture has been designed to support commercial environments as well as the more stressful operating conditions of rugged convection and conduction cooled environments.

QuiXilica V5 in the System Application Context

The efficiency of the QuiXilica V5 Architecture is best observed in the context of classical sensor I/O data processing applications. These applications generally consist of a number of sensor inputs, such as ADCs, which produce a set of digitized data streams followed by a number of processing stages. Multiple sensors may be utilized to digitize data from receivers spread in physical distance or to achieve processing gain through channel combining. Each stage of processing typically aims to reduce the data rate through signal processing until a manageable low rate data stream can be provided to the user for analysis.

This process, shown in **Figure 4** can be conceptualized as a funnel with a large number of sensors providing input data streams that are gradually reduced using a number of processing stages. At the bottom of the funnel, processed data is output after having been processed and combined to a manageable rate. This signal processing architecture is typical for beamformers and front-end sensors used in SIGINT and ELINT applications.

In such systems, there is typically a need to interconnect various heterogeneous processor types to address the changing data processing demands as data flows through the system. At the front end of the system (Stage 1 / Stage 2), data volumes and bandwidths are high but signal processing algorithmic complexity is comparatively low. Here, FPGAs can efficiently exploit multiple simple, regular parallel processing engines to deal with these initial steps. As data flows towards the bottom of the funnel to Stage 3, algorithmic complexity tends to increase and data bandwidths reduce. Traditional multicomputer architectures (e.g. Pentiums or PowerPCs) now take the lead since they allow for easy programming of the complex algorithms and have sufficient capacity to cope with the reduced data rates.

It is therefore crucial to design the system processing engines to allow these heterogeneous processing types to efficiently interconnect. Otherwise, the additional processing capacity provided by using the latest FPGA or processor is wasted.

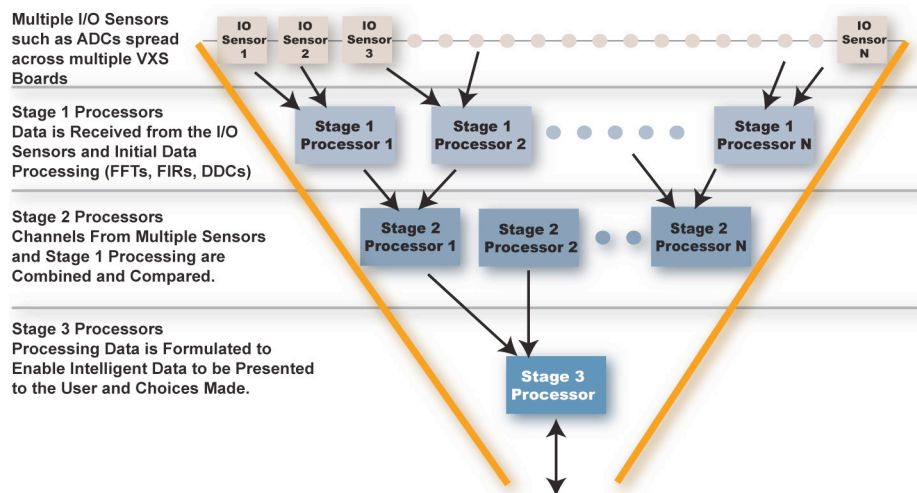


Figure 4 - Typical Sensor 'Funnel' Processing Architecture

The QuiXilica V5 products can perform the first two stages of the processing shown in **Figure 4** and to provide the bandwidth and means to transport high bandwidth data to Stage 3 processors. QuiXilica V5 digitizer boards accommodate a range and number of analog sensors, providing data to a pair of FPGAs and DDR3 SDRAM undertaking the first stage of signal processing. Using high bandwidth parallel I/O links, data is passed to the stage 2 processors for further FPGA processing .

Upon completion of this stage, data from multiple QuiXilica V5 digitizers may need to be transported to Stage 3 and further processing. Utilizing either high-speed backplane or SFP/ QSFP wired connections; data can be efficiently passed to other processors in the same enclosure or externally using open standard protocols providing a scalable and flexible architecture for sensor I/O processing applications.

Figure 5 below shows where a board based on the QuiXilica V5 Architecture might fit in the system context. All of the features required to provide interconnection of multiple boards or to interconnect to third party heterogeneous processors are implemented in this complete system solution.

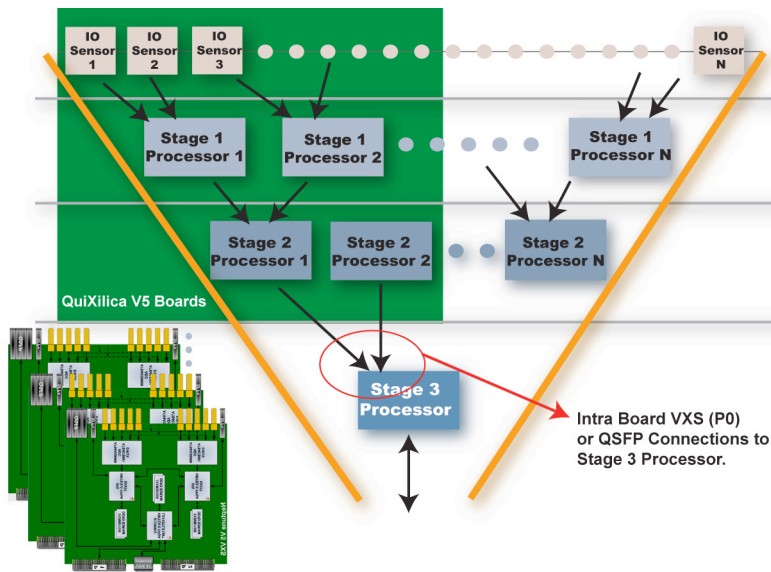


Figure 5 - Scalable QuiXilica V5 Architecture

Summary

The scalable, configurable QuiXilica V5 Architecture has been designed using the latest FPGA based processing, memory, and communications technologies available. Full ruggedization has been designed into the architecture from the outset, offering availability of products for use in harsh demanding environments for deployed systems.

Firmware and application support is provided to enable users to easily tailor the board to meet their specific design requirements.

QuiXilica V5 has been developed to meet the requirements of data-flow sensor I/O applications making QuiXilica V5 VXS boards the ideal solution for the latest generation of front-end sensor processor development.