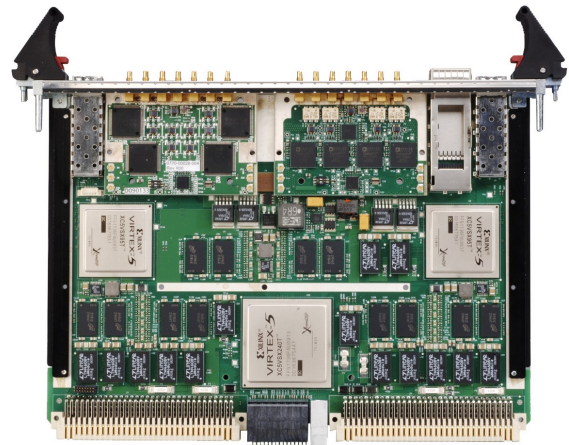


Titan-V5 VXS

Maximum FPGA Density
 Combined with High Performance
 Mixed Signal Technology.
 Without Compromise.



Features

Benefits

Eight Channels: Four 12-bit ADC Inputs at 1 GSPS each, Four 14-bit DAC Output at 1.2 GSPS each	Achieves Ultra Low Latency From Acquisition to Response Critical to Jamming and Radar Decoy Applications
First COTS Product to Achieve This Level of Performance.	Unprecedented Capability for Developers Requiring Ultra Wide Band Signal Generation
Sample Accurate Synchronization Across Multiple Boards	Enables Solutions for New Multi-channel Applications
ADC and DAC Can Use Common Clock	Synchronization Across Multiple Boards or Independent Clocks
Six Digital IO Channels Running at Up to 3.75 Gb/s Using One QSFP and Two SFP+ Front Panel Connections	Flexible Data Movement Across the Front Panel For Use in Standard VME64 Environments
Dual 4x Full Duplex VXS Links and Two Full Duplex VITA 41.6 Ethernet Links	Enhanced VXS Capability
Three Xilinx Virtex®-5 FPGAs: LXT, SXT or FXT for Each Location	Matched FPGA Processing and Analog Data Bandwidth for Dense Channel-count Systems
Three GB DDR3 SDRAM Memory, (one GB per FPGA as 2, 512 MB, 64-bit banks)	Large Memory Resources for Application Flexibility
Advanced Temperature & Current Monitoring	Protection From Damage and Usable in Customer Applications
Comprehensive Developer's Kit Provided Including FPGA Interface Cores, QuiXtart FPGA Utilities, Software and Reference Design	Faster Application Development
Convection or Conduction Cooled Options	Ruggedization Designed in For Demanding Deployed Applications

Overview

The QuiXilica Titan-V5 VXS is a 6U ANSI/VITA 41 (VXS) compliant high-speed digitizer board combining high density FPGA processing with four 12-bit A/D input channels at 1 GSPS (Gigasamples per second) and four 14-bit D/A output channels at 1.2 GSPS.

By employing three Xilinx Virtex-5 FPGAs, Tekmicro's Titan-V5 offers unmatched FPGA processing density per channel making it ideal for high channel count signal processing in applications.

Titan-V5 Reduces System Size by 50%

The Titan-V5 includes four 1.0 GSPS analog input channels, four 1.2 GSPS analog output channels, and three Xilinx Virtex-5 FPGAs, providing up to 2,336 DSP slices and 1.3 TeraMAC/s of signal processing. Having ADC and DAC channels on a single board with high-density FPGA processing, Titan-V5 can reduce the number of boards in a system by up to 50%.

Titan-V5 transfers full sensor-rate data from the ADC processing (signal capture) to the DAC processing (waveform generation). This is an ideal solution for EW applications such as jammers and Radar decoys.

The Titan-V5 features high bandwidth, low latency interconnect paths between its FPGAs. These have been carefully specified to ensure that data from the ADC input can be routed to the DAC output in support

of low latency applications. Synchronization of ADC and DAC sampling on a single board, and on multiple boards, is done using an external trigger signal. This offers significant throughput advantages for a range of advanced processing algorithms including multi-channel algorithms found in applications such as direction finding, STAP (Space Time Adaptive Processing) Radar, EW (jamming) and Synthetic Aperture Radar (SAR) Image Formation.

The Titan-V5 is available for a wide range of operating environments including commercial grade, rugged air, and conduction cooled to support deployed applications such as unmanned airborne, naval and ground vehicles. For more details see Tekmicro's Rugged Data Sheet.

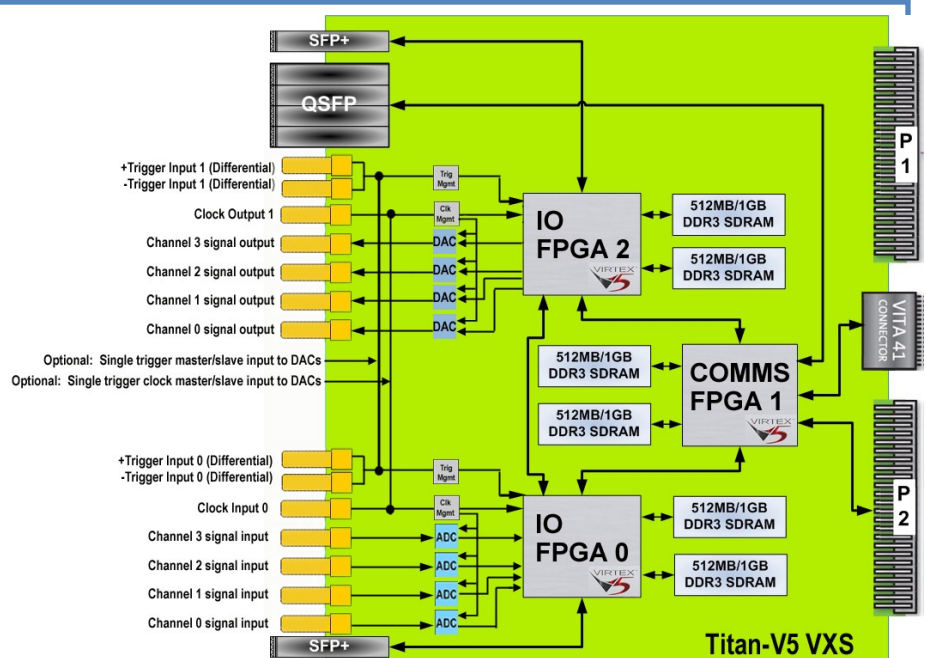
In addition to Titan-V5, Tekmicro offers a broad range of Xilinx Virtex-5 based streaming I/O and FPGA processing solutions for both analog and digital I/O in a range of form factors.

Titan-V5 VXS Details

ADC

Four channels of 1.0 GSPS, 12-bit resolution analog to digital conversion is provided on the Titan-V5. The input is single-ended, AC coupled with a full scale input level of 10 dBm (2.0 V p-p) into 50 ohms.

Titan-V5 Configuration



DAC

Four channels of up to 1.2 GSPS, 14-bit resolution digital to analog conversion is provided using the Analog Devices' AD9736. The output is single-ended, AC coupled. Maximum full scale output is 4.5 dBm (1.1 V p-p) into 50 ohms.

Virtex-5 FPGAs

Xilinx Virtex-5 FPGAs are the heart of the Titan-V5. The FPGAs interface between the ADC's, memory and I/O resources to provide a platform for implementing high performance real time processing. The Titan-V5 is configured with two SX95T FPGAs and one LX110T FPGA. An LX220T, SX240T, or FX100T FPGA can be selected to match resources to the application. All FPGAs are interconnected by wide parallel LVDS busses and via high speed serial links using the Xilinx Rocket IO MGTs.

Front Panel High Speed Serial IO

Two SFP+ sites and one QSFP site are provided on the front panel which utilize standard fiber optic or 1000BaseT modules providing physical layer support for standard protocols such as Gigabit Ethernet, Serial FPDP (ANSI VITA 17.1 & 17.2), and Fibre Channel.

VXS Backplane High Speed Serial IO

The Titan-V5 can be used as a VITA 41.0 payload card. Up to eight high speed serial links of up to 3.125 Gb/s full duplex data rates are supported via VITA 41.0 MultiGig RT2 P0 connector. Custom or standard communication protocols can be run over these links by providing appropriate firmware in the FPGA.

QuiXstart FPGA Configuration

A number of options are available for configuring the FPGA on the Titan-V5. A JTAG connection is available to allow users to configure the FPGA via standard Xilinx development tools. On board flash is available and can configure the FPGA on power up. Tekmicro's QuiXstart tool supports flexible configuration of the FPGA through a Gigabit Ethernet link from a remote server after a power up or reset event.

Trigger

Trigger input connections are provided on the front panel to allow the hardware to be employed in a variety of Radar and EW scenarios. The trigger inputs

are LVDS (LVPECL is a factory build option). One trigger input serves the DAC channels, and a second serves the ADC channels, or a single trigger input can be used for all eight analog IO channels. The trigger inputs may be used to synchronize multiple Titan-V5 boards to within a single sample period.

Clock

One clock input serves the four ADC channels, and a second clock input serves the four DAC channels, or all eight analog IO channels may be clocked from a single clock input (factory build option). The minimum input clock level is -6 dBm into 50 ohms.

Memory

The Titan-V5 has two independent banks of on board double data rate (DDR3) SDRAM for each FPGA, providing a capacity of 512 MB in each bank, 1 GB total per FPGA. The on board memory can be clocked at rates up to 400 MHz, 800 MHz double data rate.

System Monitoring

The Titan-V5 includes facilities to monitor current and temperature at various points on the board. Current monitoring of all main power rails is available. Die temperature monitoring of the three FPGAs and temperature monitoring of three locations on the PCB is also available. This allows a first level of protection when the Titan-V5 is operating in different environmental scenarios. The output from the sensors is available to users' FPGA firmware applications, to allow the user application to adapt to changes in environmental conditions. The Titan-V5 also uses the system monitoring sensors to implement a system protection mechanism which will, independently of the users' application, prevent excessive current or temperature from damaging the board.

PERFORMANCE SPECIFICATIONS

A/D Converter

Quantity: 4

Sampling Rate: 1.0 GSPS

Resolution: 12-bits

Type: Non Disclosure

Bandwidth: Up to 3rd Nyquist (1.5 Ghz)

D/A Converter

Quantity: 4

Sampling Rate: 1.2 GSPS

Resolution: 14-bits

Type: Analog Devices AD9736

Bandwidth: 1st Nyquist

Front Panel Analog Signal Input and Output

Quantity: 4 ADC and 4 DAC SSMC Connectors

Type: LVDS Termination: LVDS 100 Ω differential terminated. (LVPECL as factory build option)

Mode: Optional Independent trigger inputs for ADC's and DAC's

Master/Slave: Single common trigger for both ADC and DAC

Front Panel Trigger Inputs

Quantity: 1 or 2 via (2 or 4) SSMC Connectors

Type: LVDS Termination: LVDS 100 Ω differential terminated. (LVPECKL as factory build option).

Mode: Optional Independent trigger inputs for ADCs and DACs

Master/Slave: Single common trigger for both ADC and DAC

External Clock

Quantity: 1 or (2) via (2) SSMC Connectors

Single ended 50 Ω terminated

Input Power Range: 6 dBm (min) to 8 dBm (max)

Operating Modes: Clock Standalone / Master/Slave.

Standalone: Use independent clock inputs for ADC and DAC inputs.

Master/Slave: Single common clock distributed to ADC and DAC

Contact factory for additional performance details.

Front Panel Analog Signal Output

Type: Single-Ended Full Scale. 1.5Vpp or 2.25Vpp programmable.

Resolution: 16-bits

Memory

DDR3 SDRAM (2 banks per FPGA)

Size: (STD): 512 MB per bank, 1 GB total per FPGA

Bus: Width: 64 bits

Speed: 400 MHz, 800 MHz double data rate

Front Panel High Speed Serial Interface

2x SFP+ Ports: Providing (2) high-speed serial connections. Range of standard protocols, including Gigabit Ethernet and FibreChannel. Firmware supplied at additional cost.

1x QSFP Port: A quadruple SFP connector, of four independent lanes of high-speed serial. The lanes may be bonded together. The port supports a range of standard protocols: Gigabit Ethernet, FibreChannel and 10-Gigabit Ethernet (via 4-lane XAUI). Firmware supplied at additional cost.

JTAG Port

Access to Virtex-5 FPGAs is available via custom JTAG cable assembly that interfaces with the JTAG programming cable.

Size: Standard 6U VMEbus board, single slot; PCB: 160mm (6.3") x 233.5mm (9.2") Option: VXS P0 connector for backplane I/O

Power: +5V, +3.3V, \pm 12V from VME64 backplane. Power consumption is dependent on customer application. Power estimating available on request.



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