

Calypso-V5 VXS

Extreme Signal Acquisition and
FPGA-based Processing. Without
Compromise.



Features

Benefits

Two 12-bit ADCs at 3.2 GSPS	Fastest 12-bit sampling in a COTS product
Also supports 6 channels @ 1.6 GSPS	Best solution available for 1 st and 2 nd Nyquist sampling with > 500 MHz staring bandwidth
Three Xilinx Virtex®-5 FPGAs	Acquisition and processing on a single card without backplane throughput limitations
Single-ended or differential inputs	Works with a range of RF receiver outputs
Sample-accurate differential trigger input	Supports coherent processing of a large number of channels across multiple cards
Common or independent clock and trigger inputs for each channel group	Simplifies external clock distribution while preserving flexibility
Network interconnect through front panel SFP+ links, VITA 41.6 backplane, and P2 RTM	Supports control plane via Gigabit Ethernet with all types of VME and VXS backplanes
High speed serial I/O through front panel Quad SFP, VXS P0, and VXS RTM	High speed data plane interconnect in both VME (3.2 GB/s max) and VXS (5.7 GB/s standard, 9.8 GB/s max) applications
Six GB DDR3 SDRAM Memory	Stores large amounts of data in real-time
Advanced temperature & current monitoring	Protects card from damage and enables pro-active health monitoring
Comprehensive Developer's Kit provided including FPGA interface cores, QuiXstart FPGA utilities, software and reference designs	Lowers development risk and accelerates time to market for user application
Convection or conduction cooled options	Leverages user firmware across laboratory and deployed missions

Overview

The QuiXilica Calypso-V5 VXS is a 6U VME and ANSI/VITA 41 (VXS) compliant high-speed digitizer board that combines high density FPGA processing with the latest 12-bit ADC technology. In interleaved mode, the Calypso-V5 supports two channels at sample rates up to 3.2 GSPS. In non-interleaved mode, the Calypso-V5 supports six channels at sample rates up to 1.6 GSPS with over 2 GHz input bandwidth, supporting 1st and 2nd Nyquist operation.

By employing three Xilinx Virtex-5 FPGAs, Tekmicro's Calypso-V5 combines high resolution wideband signal acquisition with onboard high density FPGA processing. The result is a single slot solution that utilizes the latest ADC technology, supports advanced signal processing of up to 16 GB/s of digitized data, and forwards the results through a VME, RACE++, VXS or front panel connection to the next processing stage.

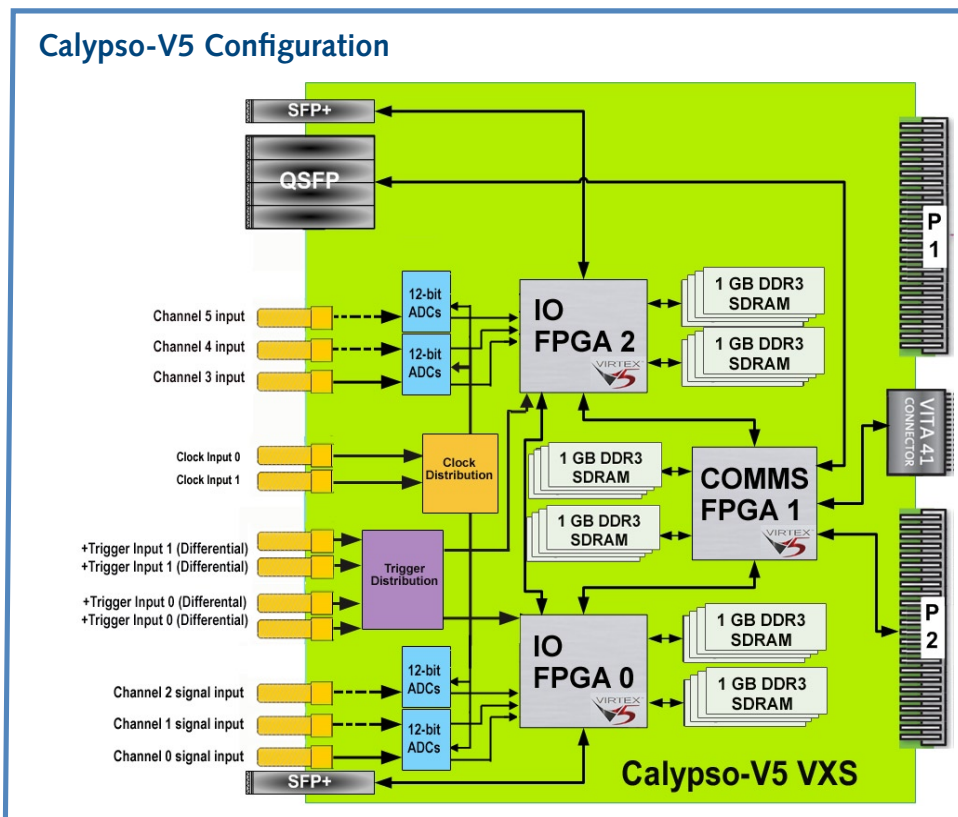
Calypso-V5 enables multi-channel signal acquisition systems with starting bandwidths of up to 1.6 GHz, with three Xilinx Virtex-5 FPGAs, providing up to 2,336 DSP slices and 1.3 TeraMAC/s of signal processing for front-end DSP.

Sample-accurate trigger synchronization of ADC sampling on a single board, and between multiple boards, is done using an external trigger signal. This offers significant advantages in terms of channel matching performance for a range of advanced processing algorithms including multi-channel algorithms found in applications such as direction finding, STAP (Space Time Adaptive Processing) RADAR, EW, ELINT and Synthetic Aperture Radar (SAR) Image Formation.

The Calypso-V5 features high bandwidth, low latency interconnect paths between its FPGAs. These have been carefully specified to ensure that data from all ADC inputs can be combined and processed together within the onboard FPGA resources, to support low-latency multi-channel applications such as adaptive beamforming.

The Calypso-V5 is available for a wide range of operating environments including commercial grade, rugged air cooled, and conduction cooled to support deployed applications such as unmanned airborne, naval and ground vehicles. For more details see Tekmicro's Ruggedization Data Sheet.

In addition to Calypso-V5, Tekmicro offers a broad range of Xilinx Virtex-5 based streaming I/O and FPGA processing solutions for both analog and digital I/O in a range of form factors.



Calypso-V5 VXS Details

ADC

The Calypso-V5 contains four advanced National Semiconductor 12-bit ADC devices, partitioned into two separate ADC groups. Within an ADC group, one ADC device is used for analog input only, and one is used for analog and trigger inputs. Each ADC device is configurable as either a single channel of 3.2 GSPS digitization or two channels of 1.6 GSPS digitization, resulting in an ADC group supporting either one analog input at 3.2 GSPS or three analog inputs at 1.6 GSPS. The analog inputs are single-ended, AC coupled into 50 ohms. As a build option, each ADC can be reconfigured with two differential, AC coupled inputs into 100 ohms (differential).

Virtex-5 FPGAs

Xilinx Virtex-5 FPGAs are the heart of the Calypso-V5. The FPGAs interface to the ADC, memory, network and I/O resources to provide a platform for implementing high performance real time processing. The standard configuration of Calypso-V5 uses two SX95T-2 FPGAs and one LX110T-2 FPGA. Alternatively, an LX220T, LX330T, SX240T, FX100T or FX200T FPGA can be selected in place of the LX110T FPGA to match resources to the application. All FPGAs are interconnected by both wide parallel LVDS busses and high speed serial links using the Xilinx RocketIO MGTs.

Front Panel High Speed Serial I/O

Two SFP+ sites and one QSFP site are provided on the front panel which utilize standard fiber optic or 1000BaseT modules providing physical layer support for standard protocols such as Gigabit Ethernet and Serial FPDP (ANSI VITA 17.1 & 17.2). Specific protocol support requires the instantiation of appropriate firmware in the FPGAs. Consult the factory for specific protocols.

VXS Backplane High Speed Serial I/O

The Calypso-V5 can be used as a VITA 41.0 (VXS) payload card. Up to eight high speed serial links of up to 3.125 Gb/s full duplex data rates are supported via VITA 41.0 MultiGig RT2 P0 connector. Standard communication protocols such as Xilinx Aurora, Serial FPDP, or PCI Express can be run over these links by providing appropriate firmware in the FPGA. Custom protocols can also be supported.

QuiXstart FPGA Configuration

A number of options are available for configuring the FPGA on the Calypso-V5. A JTAG connection is available to allow users to configure the FPGA via standard Xilinx development tools. On board flash memory is available and can configure the FPGA on power up. Tekmicro's QuiXstart tool may also be used to support flexible configuration of the FPGA through a Gigabit Ethernet link from a remote server after a power up or reset event.

Trigger

Two trigger inputs are provided on the front panel to allow the hardware to be employed in a variety of radar and electronic warfare scenarios. Each trigger input is differential, supporting inputs of ± 2.0 V, including LVDS and LVPECL. Each trigger input can serve an independent group of up to three ADC channels, or the channel groups may be configured to share a single common trigger input. The trigger is sampled at the ADC clock rate, providing sample-accurate synchronization both within a single Calypso-V5 card and across multiple cards in a system.

Clock

Two sample clock inputs are provided on the front panel, one for each ADC channel group. The input clock frequency is one-half the sample rate in interleaved mode and equal to the sample rate in non-interleaved mode, resulting in a maximum input clock frequency of 1.6 GHz in all modes. Each clock input has a minimum level of -3 dBm (nominal) into 50 Ohms. Each clock input can serve an independent group of up to 3 ADC channels, or the channel groups may be configured to share a single common clock input.

Memory

The Calypso-V5 has two independent banks of onboard double data rate (DDR3) SDRAM for each FPGA, providing a capacity of 1 GB in each bank, 2 GB per FPGA, and 6 GB total. The onboard memory can be clocked at rates up to 400 MHz, equating to 800 MT/s double data rate for throughput of 6.4 GB/s per bank.

System Monitoring

The Calypso-V5 includes facilities to monitor current and temperature at various points on the board. Current monitoring is implemented for all main

power rails. Die temperature monitoring of the three FPGAs and ADCs, and temperature monitoring of three locations on the PCB is also supported. This provides an intelligent protection and monitoring system to allow Calypso-V5 to safely cover a wide range of operational requirements in the full range of environmental scenarios. The output from the sensors is also available to users' FPGA firmware applications, to allow the user application to adapt to changes in environmental conditions. The Calypso-V5 also uses the system monitoring sensors to implement an intelligent system protection mechanism which will, independently of the users' application, prevent excessive current or temperature from damaging the board.

PERFORMANCE SPECIFICATIONS

A/D Converter

Quantity: 2 or 6 channels

Sampling Rate: 1.6 GSPS (6 channel mode), 3.2 GSPS (2 channel mode)

Resolution: 12 bits

Bandwidth: Up to 2 GHz

Front Panel Analog Signal Inputs

Quantity: 6 ADC SSMC Connectors

Type: Single ended AC coupled into 50 Ω

Build option type: Differential AC coupled into 100 Ω

Front Panel Trigger Inputs

Quantity: 2 via 4 SSMC Connectors

Type: 100 Ω differentially terminated, $\pm 2V$ input level with hysteresis of 70 mV (includes support for LVDS and LVPECL)

Mode: Independent or common for both ADC groups

External Clocks

Quantity: 2 SSMC Connectors

Type: Single ended 50 Ω terminated

Input Power Range: -3 dBm (min) to 15 dBm (max)

Operating Modes: Independent or common for both ADC groups

Memory

DDR3 SDRAM (2 fully independent banks per FPGA)

Size: 1 GB per bank, 2 GB total per FPGA

Bus Width: 64 bits per bank

Speed: 400 MHz clock rate, equating to 800 MT/s double data rate

Front Panel High Speed Serial Interface

2x SFP+ Ports: Providing (2) high speed serial connections. Range of standard protocols, including Gigabit Ethernet and Serial FPDP.

1x QSFP Port: A quadruple SFP connector, with four independent lanes of high-speed serial connections. The lanes may be bonded together. The port supports a range of standard protocols: Gigabit Ethernet, Serial FPDP and 10-Gigabit Ethernet (via 4-lane XAUI).

JTAG Port

Access to Virtex-5 FPGAs is available via custom JTAG cable assembly that interfaces with the standard Xilinx JTAG programming cable.

Size: Standard 6U VMEbus board, single slot; PCB: 160mm (6.3") x 233.5mm (9.2") Option: VXS PO connector for backplane I/O

Power: +5V, +3.3V, $\pm 12V$ from VME64 backplane.

Power consumption is dependent on customer application. Power estimation model is provided as a part of the Developers Kit.



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