

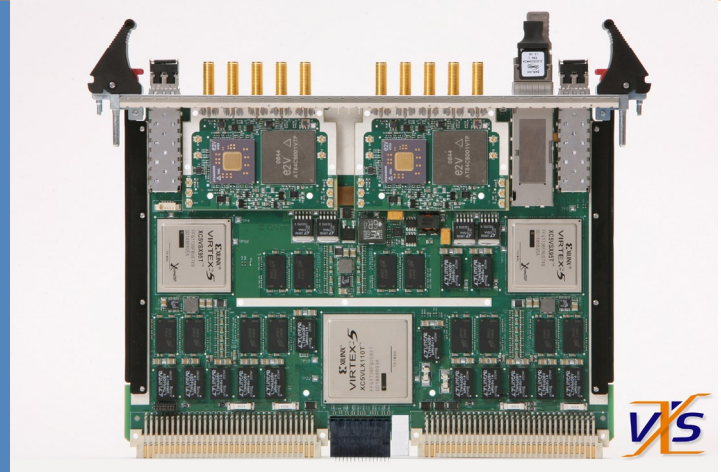
Neptune-V5 VXS

Maximum FPGA Density

Combined with High Performance

Mixed Signal Technology.

Without Compromise.



Features

Benefits

Two Channels: Two 10-bit ADC Inputs at 2.2 GSPS Each	Multichannel Output in A Single Slot
Sample Accurate Synchronization Across Multiple Boards	Supports High Channel Count Applications Such as Beam Steering With up to 144 Channels in a Single VXS chassis.
First COTS Product to Achieve This Level of Analog Signal Performance.	Unprecedented Capability for Developers Requiring Ultra Wide Band Signal Generation
Six Digital IO Channels Running at Up to 3.75 Gb/s Using One QSFP and Two SFP+ Front Panel Connections	Flexible Data Movement Across the Front Panel For Use in Standard VME64 Environments
Dual 4x Full Duplex VXS Links and Two Full Duplex VITA 41.6 Ethernet Links	Enhanced VXS Capability
Three Xilinx Virtex®-5 FPGAs: LXT, SXT or FXT for Each Location	Unmatched FPGA Processing Per Channel
Three GB DDR3 SDRAM Memory, (one GB per FPGA as two, 512 MB, 64-bit banks)	Large Memory Resources for Application Flexibility
Advanced Temperature & Current Monitoring	Protection From Damage and Usable in Customer Applications
Comprehensive Developer's Kit Provided Including FPGA Interface Cores, QuiXtart FPGA Utilities, Software and Reference Design	Faster Application Development
Convection or Conduction Cooled Options	Ruggedization Designed in For Demanding Deployed Applications

Overview

The Neptune-V5 VXS is an ANSI VITA 41-compliant dual channel high speed digitizer board based on the QuiXilica V5 architecture from TEK Microsystems. Designed to meet the needs of demanding sensor-processing applications across a range of environments, the Neptune-V5 employs three Virtex®-5 processors, advanced DDR3 SDRAM, and the latest communications technologies available. Full ruggedization has been designed into the architecture providing full support for harsh environments.

The Neptune-V5 design logically follows and meets the data flow requirements of advanced applications and does the job more efficiently than anything else available.

Widely adopted standards and the very latest in technology gives customers the optimum in performance and investment protection.

Software support for a range of open standards and protocols is provided including Gigabit Ethernet, Serial FPDP (ANSI VITA 17.1 and 17.2) and Fibre Channel. For inter-FPGA and inter-board communications, protocol support is provided for Xilinx Aurora and PCI Express.

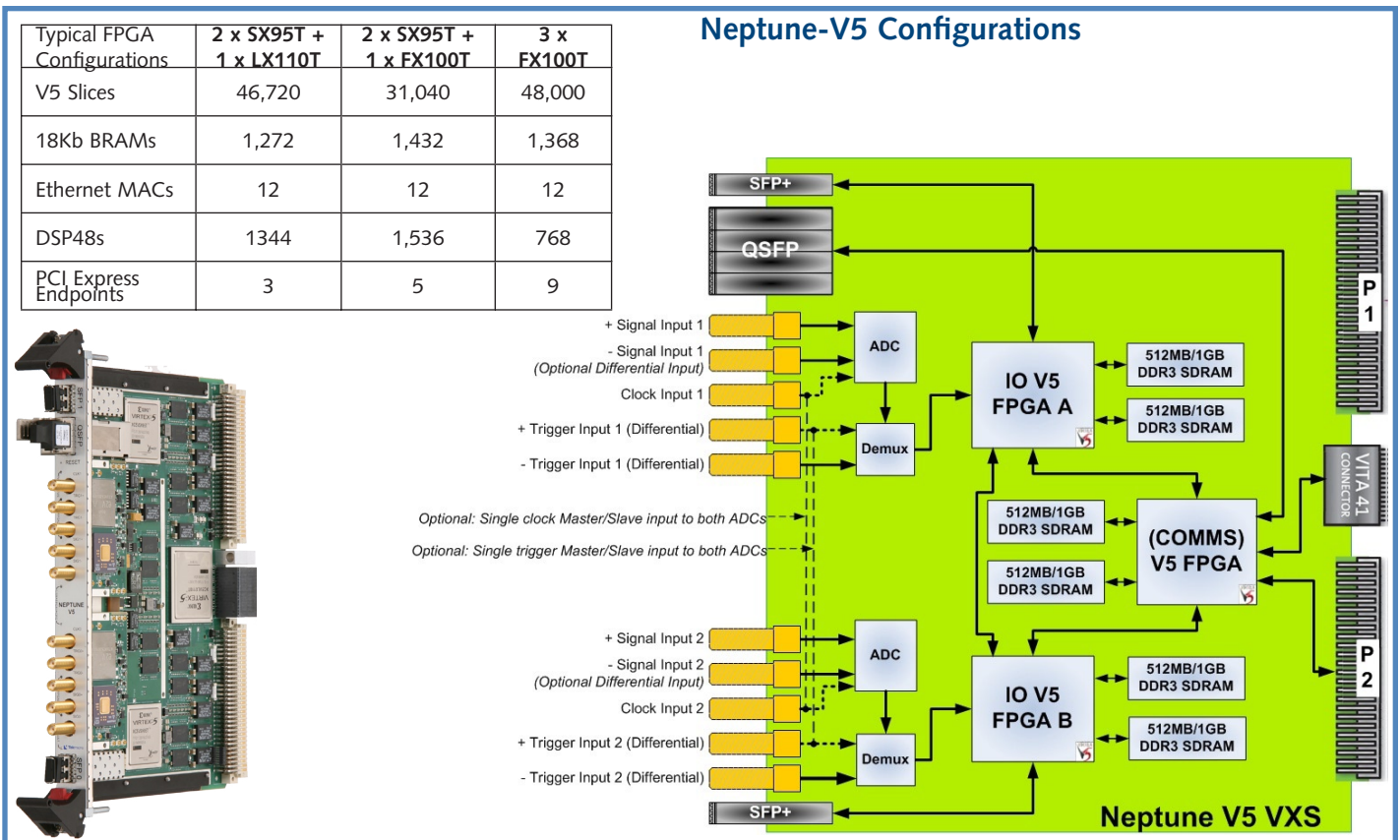
Our approach to the architecture focuses on the sensor IO processing and allows more efficient use of the three Virtex-5 processors than competitive offerings of up to seven FPGAs resulting in a lower price point and reduced power consumption.

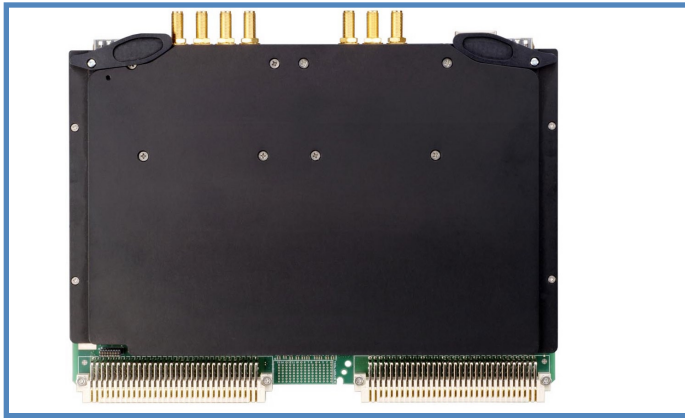
Front Panel High Speed Serial IO

The two SFP+ sites and one QSFP site on the front panel utilize standard fiber optic or 1000BaseT modules provide the physical layer support for standard protocols such as Gigabit Ethernet, Serial FPDP (ANSI VITA 17.1 & 17.2), and Fibre Channel. Alternative SFP modules can be supplied by contacting the factory.

Virtex-5 FPGAs

Xilinx Virtex-5 FPGAs are at the heart of the Neptune-V5. The FPGAs interface with the ADCs, memory and I/O resources providing the user with a platform for implementing high performance real time processing. The Charon-V5 is typically configured with two SX95T FPGAs and an LX110T. Developers can alternatively select an LX220T, SX240T, or FX100T FPGA to match resources to the application. All FPGAs are interconnected by wide parallel LVDS busses or high speed serial lanes using FPGA embedded MGTs.





Neptune-V5 meets the needs of commercial, convection, and conduction cooled environments.

In a typical configuration two Xilinx Virtex-5 SX95T FPGAs interface between the ADC's, memory and I/O resources to provide the user with a platform for implementing high performance real time processing. The IO FPGAs A and B can be any Virtex-5 FF1136 device. The back-end Comms FPGA can be any FF1136 or 1738 device which provides additional resources for implementing DSP and interfaces to the VXS backplane. All FPGAs are interconnected by wide parallel LVDS busses and also via high speed serial links using the Xilinx Rocket IO MGTs.

VXS Backplane High Speed Serial IO

The Neptune-V5 can be used as a VITA 41.0 payload card. Up to eight high speed serial links of up to 3.125 Gb/s full duplex data rates are supported via the VITA 41.0 standard MultiGig RT2 P0 connector. Custom or standard

Ruggedization Options

Specification	Commercial	Rugged Level 2	Rugged Level 3
Cooling	Convection	Convection	Conduction
Operational Temperature	0° to +55 °C (300 LFM airflow)	-40 to +70 °C (600 LFM airflow)	-40° to +85 °C (At Card Edge)
Storage Temperature	-40° to +85 °C	-55° to +100 °C	-55° to +125 °C
Relative Humidity	10% to 95% non-condensing	5% to 95% non-condensing	0% to 95% non-condensing
Conformal Coating	No	Yes	Yes
Shock	½ sine pulse, 20 g, 11 ms	½ sine pulse, 20 g, 11 ms	½ sine pulse, 40 g, 11 ms
Vibration (Sine)	2 g peak 15 to 2,000 Hz	10 g peak 15 to 2,000 Hz	10 g peak 15 to 2,000 Hz
Vibration (Random)	0.003 g ² /Hz from 15 to 2,000Hz	0.04 g ² /Hz from 15 to 2,000Hz	0.1 g ² /Hz from 15 to 2,000Hz

communication protocols can be run over these links with appropriate firmware in the FPGA.

QuiXstart FPGA Configuration

A number of options are available for configuring the FPGA on the Neptune-V5. For development purposes, a JTAG connection is available that allows users to configure the FPGA via standard Xilinx development tools. On board flash is available and can configure the FPGA on power up. Tekmicro's QuiXstart tool also supports flexible configuration of the FPGA through a Gigabit Ethernet link from a remote server after a power up or reset event.

ADCs

Two e2v AT84AS008 10-bit Analog to Digital Converters (ADCs) are provided on a Neptune-V5, each capable of operating at sampling rates of 2.2 GSPS (Gigasamples per second). The ADCs are configured as single ended AC coupled, although alternate configurations can be provided. A data ready signal output is supplied along with the data bus signals and is used to latch the data into the FPGA. Control functions on each ADC such as sampling point adjustment, gain adjustment, and input DC bias adjustment can be accessed from the FPGA, through a two-wire, I2C-compatible interface. The same interface can adjust the relative phase of the data and the data ready signal at the output of the DMUX.

High Speed Trigger Input

Trigger firmware can be implemented in the FPGA to fully synchronize data captures between multiple ADC channels on the same board or across multiple Neptune-V5 boards if required.

Memory

The Neptune-V5 has two independent banks of onboard double data rate (DDR3) SDRAM for each FPGA, providing a capacity of 512 MB in each bank, 1 GB total per FPGA. The onboard memory can be clocked at rates up to 400 MHz, 800 MHz double data rate. Optional 1 GB per bank DDR3 devices can provide a capacity of 2 GB total memory per FPGA.

System Monitoring

The Neptune-V5 board includes facilities to monitor current and temperature at various points on the board. Current monitoring of all main power rails is available. Die temperature monitoring of the three FPGAs and temperature monitoring of three locations on the PCB

is also available. This allows a first level of protection to be implemented when the Neptune-V5 is operating in a variety of different environmental scenarios. The output from the sensors will also be available to users through the Comms FPGA firmware. The condition monitoring peripherals will share an I2C bus with the I2C bus from the Comms FPGA to the QSFP module.

PERFORMANCE SPECIFICATIONS

Front Panel Analog Signal Inputs

Quantity: 1 or 2 via (4) SMA Connectors

Type: Single ended or differential.

Full Scale Input: -2dBm into 50Ω.

Input signal must be -2dBm within the first Nyquist band of the ADC to achieve full scale ADC conversion.

Front Panel Trigger Inputs

Quantity: 1 or 2 via (4) SMA Connectors

Type: LVDS (Optional: LVPECL)

Termination: LVDS 100Ω differential terminated (Optional: LVPECL)

Standalone: Independent Trigger inputs for each analog input

Master/Slave: Select Trigger MASTER, connect board-to-board connector to Trigger SLAVE

External Clock

Quantity: 1 or (2) via (2) SMA Connectors

Single ended 50Ω terminated

Input Power Range: 2dBm (min) to 10dB (max)

Operating Modes:

Clock Standalone / Master/Slave

Standalone: Use independent clock inputs for each analog input.

Master/Slave: Select clock MASTER, connect board-to-board connector to clock SLAVE

A/D Converters

Quantity: 1 or 2

Sampling Rate: 2.2 GSPS

Resolution: 10 bits

Type: e2v AT84AS008

Bandwidth: 3.3GHz at full power

Demultiplexer

Quantity: 1 or 2

Type: e2v AT84CS001

Demux Ratio: 1:4

Tunable Delay: -250ps to +250ps

Output Resolution: 10 bits

Memory

DDR3 SDRAM (2 banks per FPGA)

Size (STD): 512 MB per bank, 1 GB total per FPGA

Bus Width: 64bits

Speed: 400MHz, 800MHz double data rate

Front Panel High Speed Serial Interface

2x SFP+ Ports: Providing (2) high-speed serial connections. Range of standard protocols, including Gigabit Ethernet and FibreChannel.

1x QSFP Port: A quadruple SFP connector, of four independent lanes of high-speed serial. The lanes may be bonded together.

Port supports a range of standard protocols: Gigabit Ethernet, Fibre Channel and 10-Gigabit Ethernet (via 4-lane XAUI).

JTAG Port

Access to Virtex-5 FPGAs is available via custom JTAG cable assembly that interfaces with JTAG programming cable.

Size: Standard 6U VMEbus board, single slot; PCB: 160mm (6.3") x 233.5mm (9.2")

Power: +5V, +3.3V, ±12V from VME64 backplane. Power consumption is dependent on customer application. Power estimating tools available on request.



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