

Titan-V6 VXS

Maximum FPGA Density Combined
with High Performance Mixed
Signal Technology
Without Compromise



Features

Benefits

Eight channels: 4 12-bit ADC inputs at 1 GSPS each, 4 14-bit DAC output at 1.2 GSPS each	Achieves ultra low latency from acquisition to response critical to jamming and radar decoy applications
Sample accurate synchronization across multiple boards	Enables solutions for new multi-channel applications
ADC and DAC can use common clock	Synchronization across multiple boards or independent clocks
Twelve fiber optic interfaces running at up to 6.4 Gb/s using CXP front panel connection	Flexible data movement across the front panel for use in standard VME environments
One SFP port for Gigabit Ethernet connectivity	Network access and data movement to FPGAs via on-board Gigabit Ethernet switch
Dual 4x full duplex VXS links and 2 full duplex VITA 41.6 ethernet links	Enhanced VXS capability
Three large pin count (1759 pin package) Xilinx Virtex®-6 devices available per board (LX240, SX315, or SX475). other configurations available	Matched FPGA processing and analog data bandwidth for dense channel count systems
5 GB DDR3 SDRAM Memory	Large memory resources for application flexibility
Two fully independent banks of (72 Mb/bank) QDRII+ memory on backend FPGA	
Advanced temperature and current monitoring	Protection from damage and usable in customer applications
Comprehensive developer's kit provided including FPGA interface cores, QuiXstart FPGA utilities, software and reference designs	Faster application development
Convection or conduction cooled options	Ruggedization designed in for demanding deployed applications

Overview

The QuiXilica Titan-V6 VME / VXS is a 6U ANSI/VITA 41 (VXS) compliant high-speed digitizer board combining high density FPGA processing with four 12-bit A/D input channels at 1 GSPS (Gigasamples per second) and four 14-bit D/A output channels at 1.2 GSPS.

By employing three Xilinx Virtex-6 FPGAs, Tekmicro's Titan-V6 combines high resolution wideband signal acquisition and generation with the onboard high density FPGA processing for a range of radar and Electronic Warfare applications such as target generation, jamming, and CM / CCM techniques. The result is a single slot solution that utilizes the latest technology, supports advanced signal processing of up to 6 GB/s of digitized data, and forwards the results through VME, VXS or front panel connection via SFP+ or CXP to the next processing stage.

The Titan-V6 includes four 1.0 GSPS analog input channels, four 1.2 GSPS analog output channels, and three Xilinx Virtex-6 FPGAs, providing up to 6,048 DSP slices and 3.2 TeraMAC/s of signal processing. Having ADC and DAC channels on a single board with high density FPGA processing. The Titan-V6 transfers full sensor-rate data from the ADC processing (signal capture) to the DAC processing (waveform generation). This is an ideal solution for EW applications such as jammers and Radar decoys. Titan-V6 features high bandwidth, low latency interconnect paths between its FPGAs, these have been carefully specified to ensure that data from the ADC input can be routed to the DAC output in support of low latency applications. Synchronization of ADC and DAC sampling on a single board, and on multiple boards, is done using an external trigger signal. This offers significant throughput advantages for a range of advanced processing algorithms including multi-channel algorithms found in applications such as direction finding, Space Time Adaptive Processing (STAP) radar, EW, ELINT and Synthetic Aperture Radar (SAR) image formation.

The Titan-V6 is available for a wide range of operating environments including commercial grade, rugged air cooled, and conduction cooled to support deployed applications such as unmanned airborne, naval and ground vehicles. For more details, see Tekmicro's Ruggedization Data Sheet.

In addition to Titan-V6, Tekmicro offers a broad range of Xilinx Virtex-6 based streaming I/O and FPGA processing solutions for both analog and digital I/O in a range of form factors.

Titan-V6 VXS Details

ADC

Four channels of 1.0 GSPS, 12-bit resolution analog to digital conversion is provided using the Texas Instruments ADS5400. The input is single-ended, AC coupled with a full scale input level of 10 dBm (2.0 V p-p) into 50 Ω s.

DAC

Four channels of up to 1.2 GSPS, 14-bit resolution digital to analog conversion is provided using the Analog Devices' AD9736. The output is single-ended, AC coupled. Maximum full scale output is 4.5 dBm (1.1 V p-p) into 50 Ω s.

Virtex-6 FPGAs

Xilinx Virtex-6 FPGAs are the heart of the Titan-V6. The FPGAs interface between the ADC's, memory and I/O resources to provide a platform for implementing high performance real time processing. The Titan-V6 is configured with three high pin count Xilinx Virtex-6 devices (LX240, SX315, or SX475) per board. Other device types can be used optionally or mixed for custom configurations. All FPGAs are interconnected by wide parallel LVDS busses and via high speed Aurora serial links using the Xilinx GTX transceivers.

Front Panel High Speed Serial I/O

One 12-fiber CXP site is provided on the front panel for standard protocols such as Gigabit Ethernet or Serial FPDP (ANSI VITA 17.1 & 17.2). CXP modules and breakout cables are available optionally for flexible I/O capability.

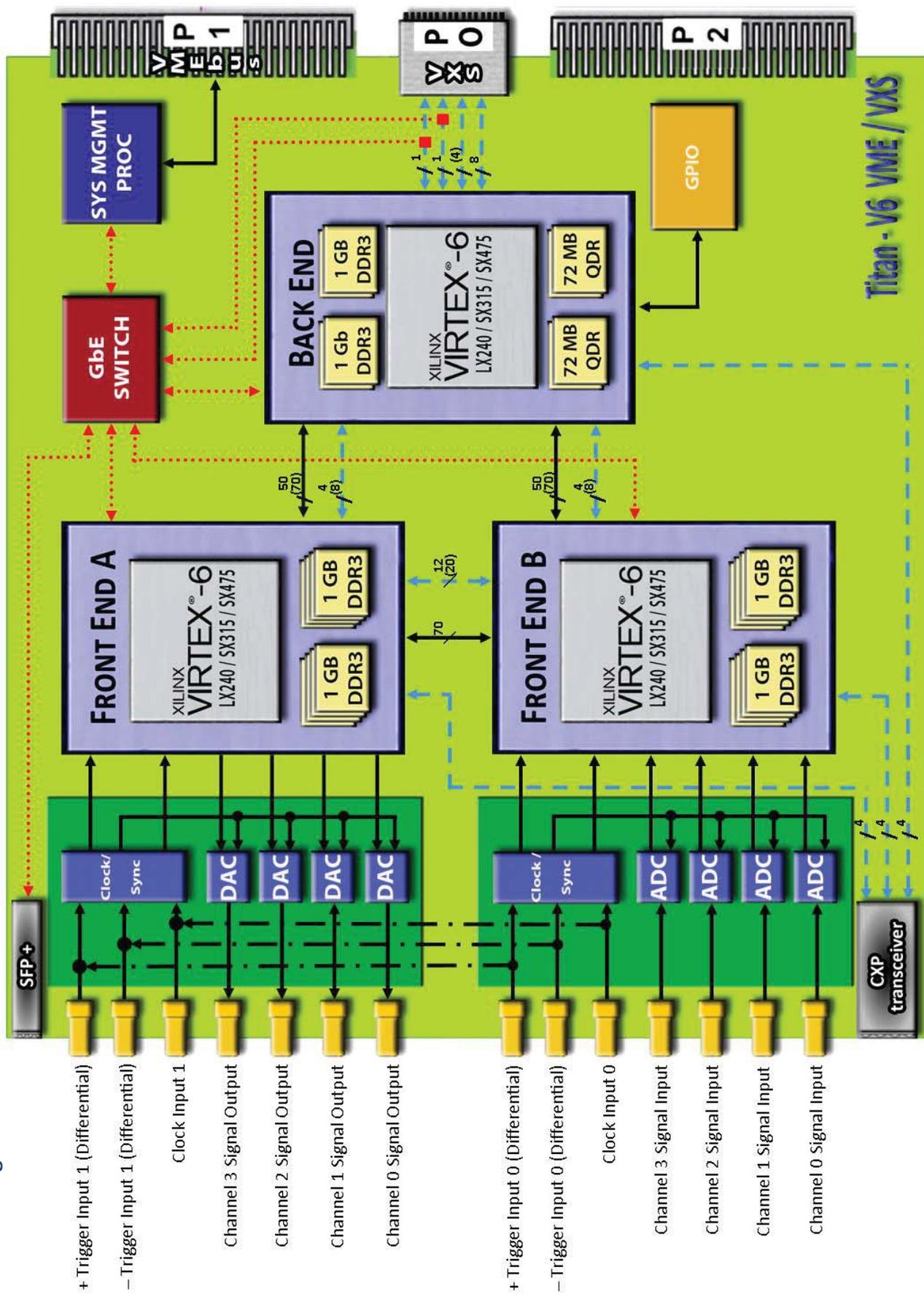
Onboard Gigabit Ethernet Networking and Switching

An onboard Gigabit Ethernet Switch connected to each FPGA supports routing of control plane signaling and minimizes FPGA involvement for data distribution/forwarding between FPGAs. A dedicated SFP port which supports both fiber and copper 1000 baseT ethernet connections is available to connect to an outside network.

VXS Backplane High Speed Serial I/O

The Titan-V6 can be used as a VITA 41.0 payload card. Up to eight high speed serial links of up to 3.125 Gb/s full duplex data rates are supported via VITA 41.0 MultiGig RT2 P0 connector. Custom or standard communication protocols can be run over these links by providing appropriate firmware in the FPGA.

Titan-V6 Configurations



— Serial (GTX links) - - - Parallel (LVDS pairs) ····· Network (GbE)

Titan - V6 VME / VXS

High Speed Parallel LVDS Interconnectivity

All FPGAs are also interconnected with a number of LVDS pairs for optimized data transfer as the block diagram shows.

QuiXstart FPGA Configuration

A number of options are available for configuring the FPGA on the Titan-V6. A JTAG connection is available to allow users to configure the FPGA via standard Xilinx development tools. Onboard flash is available and can configure the FPGA on power up. Tekmicro's QuiXstart tool supports flexible configuration of the FPGA through a Gigabit Ethernet link from a remote server after a power up or reset event.

Trigger

Trigger input connections are provided on the front panel to allow the hardware to be employed in a variety of radar and electronic warfare scenarios. The trigger inputs are LVDS (LVPECL is a factory build option). One trigger input serves the DAC channels, and a second serves the ADC channels, or a single trigger input can be used for all eight analog IO channels. The trigger inputs may be used to synchronize multiple Titan-V6 boards to within a single sample period.

Clock

One clock input serves the four ADC channels, and a second clock input serves the four DAC channels, or all eight analog I/O channels may be clocked from a single clock input (factory build option). The minimum input clock level is -6 dBm into 50 Ω .

Memory

The Titan-V6 has two independent banks of onboard DDR3 SDRAM for each FPGA. The front end FPGAs have two 1 GB banks, each with throughput of 6.4 GB/s, while the back end FPGA has two 512 MB banks, each with throughput of 3.2 GB/s. The total memory capacity is 5 GB with aggregate throughput of 32 GB/s across six banks. All DDR3 memory banks are clocked at 400 MHz for an 800 MT/s transfer rate. In addition, there are two fully independent banks of QDRII+ SRAM memory for the back end FPGA. Each QDRII+ device has a 72 Mbit capacity (144 Mbit total) supported by an 18-bit data bus per bank.

GPIO Connections

For general purpose I/O signals, the Titan-V6 can be accessed via the P2 connector and there is also an SSMC connector on the front panel which can be used for such things as a GPS signal, etc.

System Monitoring / Damage Protection

The Titan-V6 includes facilities to monitor current and temperature at various points on the board. Current monitoring of all main power rails is available through the use of a Spartan-6 FPGA. Die temperature monitoring of the three FPGAs and temperature monitoring of three locations on the PCB is also available. This allows a first level of protection when the Titan-V6 is operating in different environmental scenarios. The output from the sensors is available to the user's FPGA firmware applications, to allow the application to adapt to changes in environmental conditions. The Titan-V6 also uses the system monitoring sensors to implement a system protection mechanism which will, independently of the user's application, prevent excessive current or temperature from damaging the board.



PERFORMANCE SPECIFICATIONS

A/D Converter

Quantity: 4

Sampling Rate: 1.0 GSPS

Resolution: 12-bits

Type: Texas Instruments ADS5400

Bandwidth: Up to 3rd Nyquist (1.5 GHz)

D/A Converter

Quantity: 4

Sampling Rate: 1.2 GSPS

Resolution: 14-bits

Type: Analog Devices AD9736

Bandwidth: 1st Nyquist

Front Panel Trigger Inputs

Quantity: 1 or 2 via (2 or 4) SSMC Connectors

Type: LVDS Termination. LVDS 100 Ω differential terminated (LVPECL as factory build option)

Mode: Optional independent trigger inputs for ADCs and DACs

Master/Slave: Single common trigger for both ADC and DAC

Clock

Quantity: 1 or 2 each via SSMC Connector

Type: Single ended 50 Ω terminated

Input Power Range: 6 dBm (min) to 8 dBm (max)

Modes: Clock Standalone / Master/Slave

Network Interface

Front panel SFP for fiber or copper Gigabit Ethernet

VITA 41.6 P0 interface for 1000BASE-KX Gigabit Ethernet

Onboard Gigabit Ethernet switch

JTAG Port

Access to Virtex-6 FPGAs is available via custom JTAG cable assembly that interfaces with the standard Xilinx JTAG programming cable.

Memory

DDR3 SDRAM (2 fully independent banks per FPGA)

Size: 1 GB per front end bank, 512 GB total per back end bank

Bus Width: 64-bits per front end bank, 32-bits per back end bank

Speed: 400 MHz clock rate, 800 MT/s

QDRII + SRAM (2 fully independent banks for backend FPGA)

Size: 72Mbits per backend bank (144Mbits total)

Bus Width: 18-bits per bank

Speed: Up to 500MHz clock rate

Backplane I/O

VME Interface:

V6A - master, slave, A32:D32, A32:BLT, A32:MBLT, A32:2eSST

V6D - slave only, A32:D32, A32:BLT16

VXS Interface: P0 connector supports 8X high speed serial links on the backplane

GPIO Interface: P2 connector

Rear Transition Module (Optional): For rear access to the board, a Rear Transition Module is available that provides connections for GPIO connections, network access, PPS and trigger signals

Front Panel I/O

Gigabit Ethernet via SFP+

CXP supporting 12 fiber optic at up to 6.4 Gb/s per link

Size

Standard ANSI / VITA 1.1-1997 (R2003) VMEbus board, 6U x 4HP, single 0.8" slot

Optional VXS P0 connector for backplane I/O

Power

+5v, +3.3V, \pm 12V from backplane. Power consumption is dependent on customer application. Power estimation Model is provided as part of the Developers Kit.

Contact factory for additional performance details.



Environmental / Ruggedization

In addition to providing high performance, Tekmicro boards and systems have been designed for ruggedization and power management. Tekmicro products operate effectively in laboratory, rugged air-cooled, and rugged conduction-cooled environments to meet the needs of deployed applications.

Ruggedization Options

Specification	Commercial	Rugged Level 2	Rugged Level 3
Cooling	Convection	Convection	Conduction
Operational Temperature	0 to +55 °C (300 LFM airflow)	-40 to +70 °C (600 LFM airflow)	-40 to +85 °C (At Card Edge)
Storage Temperature	-40 to +85 °C	-55 to +100 °C	-55 to +125 °C
Relative Humidity	10% to 95% non-condensing	5% to 95% non-condensing	0% to 95% non-condensing
Conformal Coating	No	Yes	Yes
Shock	½ sine pulse, 20 g, 11 ms	½ sine pulse, 20 g, 11 ms	½ sine pulse, 40 g, 11 ms
Vibration (Sine)	2 g peak 15 to 2,000 Hz	10 g peak 15 to 2,000 Hz	10 g peak 15 to 2,000 Hz
Vibration (Random)	0.003 g ² /Hz from 15 to 2,000 Hz	0.04 g ² /Hz from 15 to 2,000 Hz	0.1 g ² /Hz from 15 to 2,000 Hz



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