

## Quixilica Janus VXS



The Quixilica Janus VXS is part of the Quixilica VXS family of FPGA based processing hardware. The Quixilica VXS family provides a complete range of flexible analog and digital IO products in the VITA 41.0 VXS form factor. The Quixilica family couples high performance analog and digital IO front ends with a scalable FPGA based processing architecture. Memory and inter-processor communications resources have been optimized to address the requirements of very high performance real time digital signal processing applications. The Quixilica family is supported by a range of development kits, FPGA cores and software, providing users with power and flexibility while retaining consistency and ease of use.

Key applications for the Janus VXS include radar, electronic warfare, software radio, automatic test equipment, scientific instrumentation and telecommunications.

### Hardware Description

The Janus VXS is a 6U form factor card that can be employed as a payload card as defined in the VITA 41.0 VXS specification. The card can also be deployed in a standard VME 64 chassis if the P0 connector is not populated. The VME 64 interface is used only for powering the card - the VME bus interface itself is not implemented. Control and high speed data IO for the card is implemented using the

- 7 x 16-bit 500 MSPS DAC channels, based on MAX5891
- Xilinx XC2VP70 FPGA
- VME/VXS form factor, VITA 41.0 compliant, 8 x 3.125 Gbps serial I/O links
- 2 x front-panel SFP slots for 2.5 Gbps fiber or copper transceivers
- 2 x on-board DDR SDRAM banks, 512 MB per bank
- 2 x DDR SDRAM SODIMM slots, up to 2 GB each
- Quixstart flexible FPGA configuration system
- Developer's Kit available, containing FPGA interface cores, software and reference design

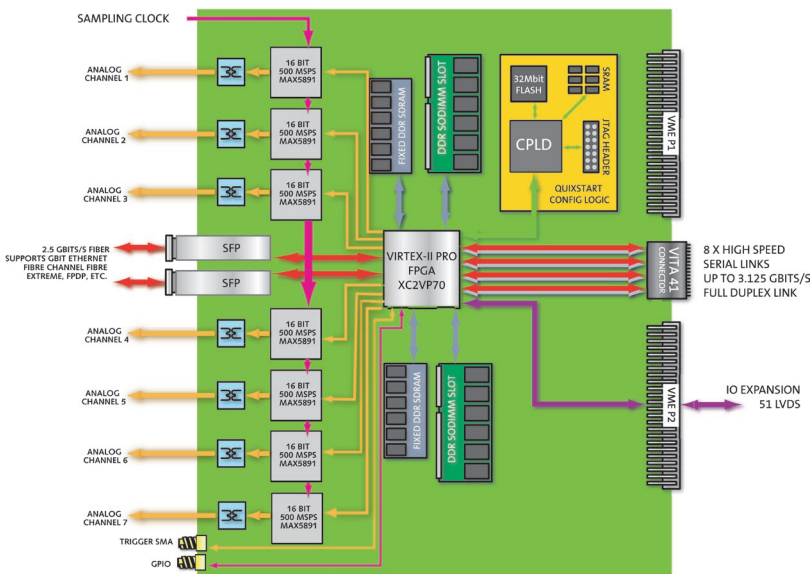
high speed serial links available on the front panel and/or the backplane P0 connector. The card can also be used standalone (i.e. without a backplane).

The Janus VXS is supplied with a standard FPGA bitstream and Windows based software application for a multi-channel, arbitrary waveform generator. A standard Gigabit Ethernet link to the front panel is used to interface the card to the host PC.

A hardware reference manual provides sufficient detail to develop FPGA based applications for the card entirely from scratch. However, for rapid development, an additional Developer's Kit can be purchased which contains FPGA interface cores, software and source code for the arbitrary waveform generator system as a reference design.

### FPGA

A Xilinx Virtex-II Pro XC2VP70 FPGA is at the heart of the Janus VXS product. The FPGA provides interfacing between the DACs, memories and IO resources on the card as well as providing the user with a platform for implementing high performance real time processing.



Janus VXS Block Diagram

The P70 FPGA provides two embedded PPC 405 processors and 16 Rocket IO high speed serial multi Gbps transceivers. The Rocket IO links are the principal mechanism used for high speed data IO and control of the Janus VXS card.

### Digital to Analog Converters

Seven channels of 500 MSPS, 16 bit resolution digital to analog conversion are provided on the Janus VXS. The output channels are based around the MAXIM MAX5891 part. The outputs are AC coupled. Full scale output voltage is -2dBm with a 50 ohm double-terminated load. All channels are simultaneously clocked with a 50 ohm, single ended clock input. The layout has been carefully designed to ensure phase matching of the clock across all channels. Trigger input and output connections are provided on the front panel to allow the hardware to be employed in a variety of typical radar and EW scenarios. Trigger firmware can be implemented in the FPGA for maximum flexibility.

### Memory

Two banks of onboard double data rate SDRAM memory are provided on the Janus VXS interfaced to the FPGA. DDR memory allows data to be read or written on both the rising and falling edges of the clock. Currently, 0.5 GB per bank is provided with the memory arranged to have a 64 bit wide data bus. Deeper memories of up to 1 GB per bank will be offered when higher capacity memory parts are released.

The Janus VXS also provides two independent SODIMM sites for Double Data Rate (DDR) SDRAM modules, interfaced to the FPGA. The SODIMM modules support 64 bit wide data transfers. Standard SODIMM modules up to 1 GB are currently available and users can either purchase their own modules or specify the memory they require as additional cost items to be fitted to the Janus VXS card prior to delivery.

Memory interface cores for the DDR memory are available for the FPGA as part of a Developers Kit (see below). These

cores implement all of the complex memory control circuitry and provide the user with a simple FIFO style interface into their own application circuits in the FPGA.

### Front Panel High Speed Serial IO

Two SFP sites are provided on the front panel of the Janus VXS. These can be populated with commercially available fiber optic or copper SFP modules. These modules provide physical layer support for standard protocols such as Gigabit Ethernet, InfiniBand and Serial FPDP.

SFP modules for short wave fiber, long wave fiber or copper (e.g. Gigabit Ethernet) can be supplied and fitted if required. Contact the factory to discuss special requirements.

### VXS Backplane High Speed Serial IO

The Janus VXS can be used as a VITA 41.0 payload card. Up to 8 high speed serial links of up to 3.125Gbit/s full duplex data rates are supported via the VITA 41.0 standard MultiGig RT2 P0 connector. Different custom or standard communication protocols can be run over these links by providing appropriate firmware in the FPGA.

Population of the VITA 41.0 P0 connector is a build option that must be specified if the user wishes to deploy the high speed serial links on a backplane. Other hardware and firmware products in the Quixilica family and from third party vendors are available to aid rapid implementation of complete VXS systems. It is recommended that users should contact the factory to discuss system requirements if they are considering using the high speed serial connections on the Janus VXS.

### P2 Connector GPIO

Up to 32 LVDS differential pairs, or 64 single ended GPIOs from the FPGA are available on the P2 expansion connector. Sufficient information is supplied in the Janus VXS hardware manual for users to develop fully custom transition cards for their application if required.

### Janus Analog Performance

Analog full scale output level	-2dBm
-3dB bandwidth	150kHz to 425 MHz
Resolution	16 bits
SFDR to Nyquist	TBD
Coupling and termination	AC coupled, 50 ohm
Output connector	SMA female 50 ohm
Clock input level	-10 dBm to +10dBm
Clock input frequency	<500 MHz
Clock input connector	SMA female 50 ohm
Channel to channel matching	30 ps

### Quixstart FPGA Configuration

A number of options are available for configuring the FPGA on the Janus VXS. For development purposes, a JTAG connection is available that allows users to configure the FPGA via standard Xilinx development tools such as Impact and Chipscope. When a stable design is available, an on board flash memory can be programmed with the final bitstream and the FPGA will configure on power up. The Quixstart configuration mechanism also supports flexible configuration or reconfiguration of the FPGA through a Gigabit Ethernet link. The Janus VXS can be set up to fetch its configuration from a remote server after a power up or reset event. This is useful for applications where different bitstreams may be used to run the board in different modes. It is also suitable for applications where remote bitstream reconfiguration is required or where it is undesirable to have bitstreams held in on-board flash due to security considerations.

The setup files and software required for the full Quixstart system are supplied as part of the Developer's Kit.

### Software Support

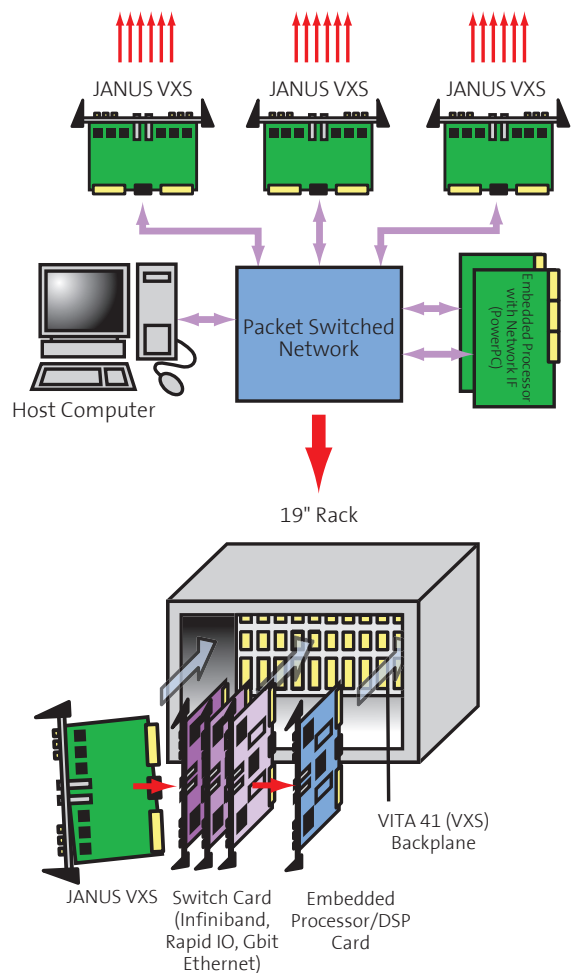
The Janus VXS is supplied with a bitstream and executable Windows GUI application for an arbitrary waveform generator system. This provides users with a mechanism to experiment with and verify correct operation of the card. To use the application, users will require a host PC equipped with a Windows 2000/XP operating system and a fiber optic Gigabit Ethernet interface.

A UCF file for the FPGA and a detailed hardware reference manual is provided to allow users to implement their own FPGA designs.

### Recommended Development Tools

The following development tools are required / recommended for use with the Janus VXS if users are developing their own FPGA designs for the card:

- Xilinx ISE
- Xilinx Chipscope software (recommended for on chip hardware debugging)
- Xilinx Parallel IV or USB JTAG download cable
- Simulation / Synthesis tools as preferred by the user. (if not using Xilinx XST)
- Xilinx EDK (Required if developing for embedded PPC 405 cores in FPGA)
- Microsoft Visual C++ (if using Application Developer's Kit)



### Janus VXS Application Developer's Kit

To aid rapid development of user FPGA designs for the Janus VXS, it is recommended that the additional Application Developer's Kit for the Janus VXS is purchased.

This kit provides the following items:-

- Quixilica Quixstream UDP/Gigabit Ethernet FPGA Cores host software (Windows and LINUX)
- DDR SDRAM FIFO Interface FPGA Cores
- Setup files and instructions for Quixstart FPGA configuration system
- Reference design - Source code for arbitrary waveform generator system firmware and software
- User manuals for all of the kit components and reference design

### Signal Processing Cores

A complete range of high performance signal processing cores is available as part of the Quixilica family, including floating point arithmetic, programmable FIR filters, Digital Receivers, FFTs and QR Decomposition. Customization or development of IP for specific applications is also possible. Contact factory for availability of IP and targeted Application Developer's Kits for radar and EW applications.

### Quixtream Cores/Software for High Speed Interconnect

Tekmicro continues to develop support for other standard communications protocols as part of the Quixtream family. Contact us for cores and software to support InfiniBand, Serial FPDP, Fibre Channel, Aurora, USB 2 and more.

### Ordering Information

Janus VXS 6U VME DAC Card

Part Number: Qx-Janus-VXS-A-P-N

P = P0 MultiGig RT2 Connector Build Option

Y => Fit P0 Connector (For use in VXS Chassis)

N => Don't Fit P0 Connector (For use in VME 64 Chassis)

Xilinx XC2VP70-6C Devices fitted as standard

Contact factory for following optional items:

- Alternative FPGA speed grades and/or industrial silicon variants
- Supply of DDR SODIMM modules pre-fitted
- Availability of alternative QDR memory chips
- Supply of copper or long wave fiber SFP transceivers

### Janus VXS Application Developers Kit

Part Number: Qx-JAN-DK01-DL

Contact factory for availability of additional DSP cores and Quixtream interconnect cores.

### Specifications

Mechanical	6U x 160mm x 4HP (standard VMEbus, single slot)
Power Requirements (max)	+5V 7A +3.3V 11A +12V 2A Subject to FPGA firmware characteristics.
Operating Temperature	0° to +55°C (Commercial)
Storage Temperature	-40° to +85°C (Commercial)
Cooling Airflow	15 CFM at sea level (estimated)
Ruggedization	Contact the factory
Warranty	One year limited hardware warranty.

© Copyright TEK Microsystems, 2007

All copyright, database rights and other intellectual property rights in this Data Sheet belong to Tekmicro or its licensors and any publication of this Data Sheet requires the express licence of TEK Microsystems.

Quixilica® is a registered trademark of QinetiQ Ltd. Other products or brand names are trademarks or registered trademarks of their respective holders.



TEK Microsystems Inc  
2 Elizabeth Dr.  
Chelmsford MA 01824  
978.244.9200  
fax: 978.244.1078  
email: sales@tekmicro.com  
www.tekmicro.com