

Proteus-V6 VXS

Extreme Signal Acquisition
and FPGA-based Processing
Without Compromise



Features

Benefits

Two 10-bit ADCs at 5 GSPS	Fastest 1 st Nyquist sampling in a COTS product
Also supports 4 channels @ 2.5 GSPS or 8 channels @ 1.25 GSPS	Implements multi-channel systems in fewer slots
Three large pin count (1759 Pin Package) Xilinx Virtex [®] -6 devices available per board (LX240, SX315, or SX475) Other configurations available	FPGA processing resources to match application requirements
Single-ended or differential inputs	Works with a range of RF receiver outputs
Sample-accurate differential trigger input	Supports coherent processing of a large number of channels across multiple cards
Five GB DDR3 SDRAM memory	Large memory resources for application flexibility
Two fully independent banks (72 Mb/bank) of QDRII+ memory on backend FPGA	
Single front panel clock input	Simplifies external clock distribution
Network interconnect through front panel SFP+ link, VITA 41.6 backplane, and P2 RTM	Supports control plane via Gigabit Ethernet with all types of VME and VXS backplanes
Twelve fiber optic interfaces running at up to 6.4 Gb/s using CXP front panel connection	Flexible data movement across the front panel for use in standard VME environments
Advanced temperature & current monitoring	Protection from damage and usable in customer applications
Comprehensive developer's kit provided including FPGA interface cores, QuiXstart FPGA utilities, software and reference designs	Faster application development
Convection or conduction cooled options	Ruggedization designed in for demanding deployed applications

Overview

The QuiXilica Proteus-V6 VXS is a 6U VME and ANSI/VITA 41 (VXS) compliant high-speed digitizer board that combines high density FPGA processing with two 10-bit ADC devices, each of which can operate either as a single channel digitizing at up to 5 GSPS; two channels digitizing at up to 2.5 GSPS; or four channels digitizing at up to 1.25 GSPS.

By employing three Xilinx Virtex-6 FPGAs, Tekmicro's Proteus-V6 combines ultra wideband signal acquisition with onboard high density FPGA processing. The result is a single slot solution that utilizes the latest ADC technology, supports advanced signal processing of up to 12.5 GB/s of digitized data, and forwards the results through a VME, RACE++, VXS or front panel connection to the next processing stage.

Proteus-V6 enables multi-channel signal acquisition systems with staring bandwidths of up to 2.5 GHz, with three Xilinx Virtex-6 FPGAs, providing up to 6,048 DSP slices and 7.2 TeraMAC/s of signal processing for front-end DSP, and can reduce the deployed size of multichannel systems by up to 50% compared to alternative solutions.

The Proteus-V6 features high bandwidth, low latency interconnect paths between its FPGAs. These have been carefully specified to ensure that data from all ADC inputs can be combined and processed together within the onboard FPGA resources, to support low-latency multi-channel applications such as adaptive beamforming.

Sample-accurate synchronization of ADC sampling on a single board, and between multiple boards, is done using an external trigger signal. This offers significant advantages in terms of channel matching performance for a range of advanced processing algorithms including multi-channel algorithms found in applications such as direction finding, STAP (Space Time Adaptive Processing) RADAR, EW, ELINT and Synthetic Aperture Radar (SAR) Image Formation.

The Proteus-V6 is available for a wide range of operating environments including commercial grade, rugged air cooled, and conduction cooled to support deployed applications such as unmanned airborne, naval and ground vehicles. For more details see Tekmicro's Ruggedization Data Sheet.

In addition to Proteus-V6, Tekmicro offers a broad range of Xilinx Virtex-6 based streaming I/O and FPGA processing solutions for both analog and digital I/O in a range of form factors.

Proteus-V6 VXS Details

ADC

Proteus-V6 contains two EV10AQ190 quad 10-bit 1.25 GSPS ADCs. Each is configurable as either a single channel of 5 GSPS digitization; two channels of 2.5 GSPS digitization; or four channels of 1.25 GSPS digitization. The inputs are single-ended, AC coupled with a full scale input level of 0 dBm into 50 Ω . As a build option, each ADC can be reconfigured with two differential, AC coupled inputs with a full scale input level of -5 dBm (nominal) into 100 Ω (differential).

Virtex-6 FPGAs

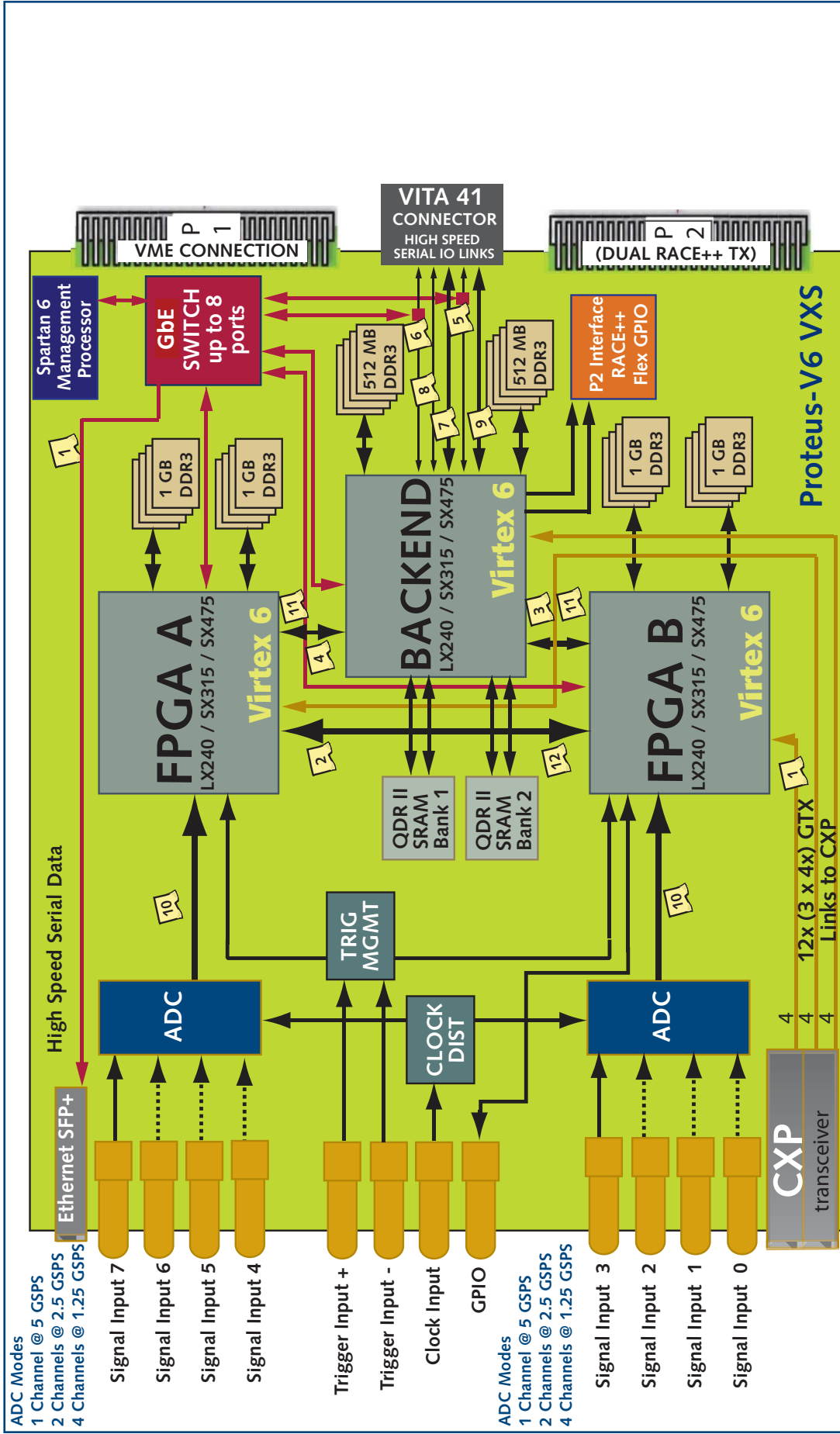
Xilinx Virtex-6 FPGAs are the heart of the Proteus-V6. The FPGAs interface between the ADC's, memory and I/O resources to provide a platform for implementing high performance real time processing. The Proteus-V6 is configured with three high pin count Xilinx Virtex-6 devices (LX240, SX315, or SX475) per board. Other device types can be used optionally or mixed for custom configurations. All FPGAs are interconnected by wide parallel LVDS busses and via high speed serial links using the Xilinx GTX transceivers.

Front Panel High Speed Serial I/O

One 12-fiber CXP site is provided on the front panel for standard protocols such as Gigabit Ethernet, Serial FPDP (ANSI VITA 17.1 & 17.2), and Fibre Channel. CXP modules and breakout cables are available optionally for flexible I/O capability.

On-Board Gigabit Ethernet Networking and Switching

An on-board Gigabit Ethernet Switch connected to each FPGA supports routing of control plane signaling and minimizes FPGA involvement for data distribution/forwarding between FPGAs. A dedicated SFP port which supports both fiber and copper Gigabit Ethernet connections is available to connect to an outside network.



ADC Modes

- 1 Channel @ 5 GSPS
- 2 Channels @ 2.5 GSPS
- 4 Channels @ 1.25 GSPS

- Signal Input 7
- Signal Input 6
- Signal Input 5
- Signal Input 4

- Trigger Input +
- Trigger Input -
- Clock Input
- GPIO

ADC Modes

- 1 Channel @ 5 GSPS
- 2 Channels @ 2.5 GSPS
- 4 Channels @ 1.25 GSPS

- Signal Input 3
- Signal Input 2
- Signal Input 1
- Signal Input 0

Notes:

1. Hardware build option for legacy mode user firmware designs of SFP to user FPGA
2. 12x Inter FPGA GTX links
3. 4x Inter FPGA GTX links
4. 4x Inter FPGA GTX links
5. Cross point switch will select whether VITA41 Port A link 0 drives FPGA directly or connects into the onboard GbE switch

Notes:

6. Cross point switch selects whether VITA 41 Port A link A drives FPGA directly or connects into the on board GbE switch)
7. 5x Additional GTX links VITA 41.11 ports
8. 2x GTX Links to VITA 41.6 / 41.11 ports on BP
9. 8x GTX links to Port A and Port B
10. 73 LVDS pairs plus clocks. Each pair can be used as 2x LVCMOS25
11. 50 LVDS pairs or 2x LVCMOS25
12. 70 LVDS pairs or 2x LVCMOS25

VXS Backplane High Speed Serial I/O

The Proteus-V6 can be used as a VITA 41.0 payload card. Up to eight high speed serial links of up to 3.125 Gb/s full duplex data rates are supported via VITA 41.0 MultiGig RT2 P0 connector. Custom or standard communication protocols can be run over these links by providing appropriate firmware in the FPGA.

QuiXstart FPGA Configuration

A number of options are available for configuring the FPGA on the Proteus-V6. A JTAG connection is available to allow users to configure the FPGA via standard Xilinx development tools. Onboard flash is available and can configure the FPGA on power up. Tekmicro's QuiXstart tool supports flexible configuration of the FPGA through a Gigabit Ethernet link from a remote server after a power up or reset event.

Trigger

Trigger input connections are provided on the front panel to allow the hardware to be employed in a variety of Radar and EW scenarios. The trigger inputs are LVDS (LVPECL is a factory build option). The trigger inputs may be used to synchronize multiple Proteus-V6 boards to within a single sample period.

Clock

One clock input serves both ADC devices. The minimum input clock level is -6 dBm into 50 Ω .

Memory

The Proteus-V6 has two independent banks of onboard double data rate (DDR3) SDRAM for each FPGA. The front end FPGAs have two 1 GB banks, each with throughput of 6.4 GB/s, while the back end FPGA has two 512 MB banks, each with throughput of 3.2 GB/s. The total memory capacity is 5 GB with aggregate throughput of 32 GB/s across six banks. All DDR3 memory banks are clocked at 400 MHz for an 800 MT/s transfer rate. In addition, there are 2 fully independent banks of QDRII+ SRAM memory for the Backend FPGA. Each QDRII+ device has a 72Mbit capacity (144 Mbit total) supported by an 18 bit data bus per bank.

System Monitoring / Damage Protection

The Proteus-V6 includes facilities to monitor current and temperature at various points on the board. Current monitoring of all main power rails is available through the use of a Spartan6 FPGA. Die temperature monitoring of the three FPGAs and temperature monitoring of three locations on the PCB is also available. This allows a first level of protection when the Proteus-V6 is operating in different environmental scenarios. The output from the sensors is available to users' FPGA firmware applications, to allow the user application to adapt to changes in environmental conditions. The Proteus-V6 also uses the system monitoring sensors to implement a system protection mechanism which will, independently of the users' application, prevent excessive current or temperature from damaging the board.



PERFORMANCE SPECIFICATIONS

A/D Converter

Quantity: 2

Sampling Rate: Up to 5 GSPS (one channel per ADC), 2.5 GSPS (two channels per ADC), or 1.25 GSPS (four channels per ADC. Up to eight total channels.)

Resolution: 10 bits

Type: EV10AQ190 from E2V

Bandwidth: Up to 3 GHz

Front Panel Analog Signal Input

Quantity: 8 ADC SMA Connectors

Type: Single ended AC coupled

ADC Full Scale Input: 0 dBm into 50 Ω .

Build option type: Differential AC coupled

Up to four differential AC-coupled inputs, with full scale input of -5 dBm into 100 Ω .

Front Panel Trigger Inputs

Quantity: 1 via 2 SMA Connector

Type: 100 Ω differential terminated, \pm 2V input level with hysteresis of 70 mV.

Includes support for LVDS (LVPECL as factory build option).

Mode: Single common trigger for both ADCs

External Clock

Quantity: 1 SMA Connector

Type: Single ended 50 Ω terminated

Input Power Range: -3 dBm (min) to 15 dBm (max)

Operating Modes: Single common clock distributed to both ADCs

Front Panel High Speed Serial Interface

12x Fiber Optic Transceivers on CXP module

Up to 6.4 Gb/s, 8B/10B or 64/66 encoding

Range of standard protocols, including Gigabit Ethernet and Serial FPDP.

Network Interface

Front panel SFP for fiber or copper Gigabit Ethernet

VITA 41.6 P0 interface for 1000BASE-KX Gigabit Ethernet.

Onboard Gigabit Ethernet switch

JTAG Port

Access to Virtex-6 FPGAs is available via custom JTAG cable assembly that interfaces with the standard Xilinx JTAG programming cable.

Memory

DDR3 SDRAM (2 fully independent banks per FPGA)

Size: 1 GB per front end bank, 512 MB per back end bank

Bus Width: 64 bits per front end bank, 32 bits per back end bank

Speed: 400 MHz clock rate, 800 MT/s

QDRII+ SRAM (2 fully independent banks for backend FPGA)

Size: 72Mbits per bank (144Mbits total)

Bus Width: 18 bits per bank

Speed: Up to 500MHz clock rate

Backplane I/O

VME Interface: D16/D32 slave interface, etc.

VXS Interface: P0 connector supports 8X high speed serial links on the backplane

GPIO Interface: P2 connector

RACE++ Interface (Optional): P2 Connector can be configured to support RACE++ environments

Rear Transition Module (Optional): For rear access to the board, a Rear Transition Module is available which provides connections for GPIO connections, network access, pps, and trigger signals

Size

Standard 6U VMEbus board, single slot

Optional VXS P0 connector for backplane I/O

Power

+5V, +3.3V, \pm 12V from backplane. Power consumption is dependent on customer application. Power estimation model is provided as part of the Developers Kit.

Contact factory for additional performance details.



Environmental / Ruggedization

In addition to providing high performance, Tekmicro boards and systems have been designed for ruggedization and power management. Tekmicro products operate effectively in laboratory, rugged air-cooled, and rugged conduction-cooled environments to meet the needs of deployed applications.

Ruggedization Options

Specification	Commercial	Rugged Level 2	Rugged Level 3
Cooling	Convection	Convection	Conduction
Operational Temperature	0 to +55 °C (300 LFM airflow)	-40 to +70 °C (600 LFM airflow)	-40 to +85 °C (At Card Edge)
Storage Temperature	-40 to +85 °C	-55 to +100 °C	-55 to +125 °C
Relative Humidity	10% to 95% non-condensing	5% to 95% non-condensing	0% to 95% non-condensing
Conformal Coating	No	Yes	Yes
Shock	½ sine pulse, 20 g, 11 ms	½ sine pulse, 20 g, 11 ms	½ sine pulse, 40 g, 11 ms
Vibration (Sine)	2 g peak 15 to 2,000 Hz	10 g peak 15 to 2,000 Hz	10 g peak 15 to 2,000 Hz
Vibration (Random)	0.003 g ² /Hz from 15 to 2,000 Hz	0.04 g ² /Hz from 15 to 2,000 Hz	0.1 g ² /Hz from 15 to 2,000 Hz



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