

Quixilica Triton VXS



- Single Channel, 2 GS/s ADC/DAC and Xilinx Virtex-II Pro FPGA Processing Engine
- 1x 10 bit 2 GS/s Atmel ADC/DMUX
- 1x 12 bit 2 GS/s Euvis MUX/DAC
- VME/VXS form factor, VITA 41.0 Compliant, 8x 3.125 Gbit/s serial I/O links
- 2x Front Panel SFP slots for 2.5 Gbit/s fiber or copper transceivers
- 2x DDR SDRAM SODIMM Slots, up to 2 GB each
- 2x On-Board DDR SDRAM Banks, 0.5 GB each
- Quixstart flexible FPGA configuration system
- Developer's Kit available with FPGA interface cores, software and reference design

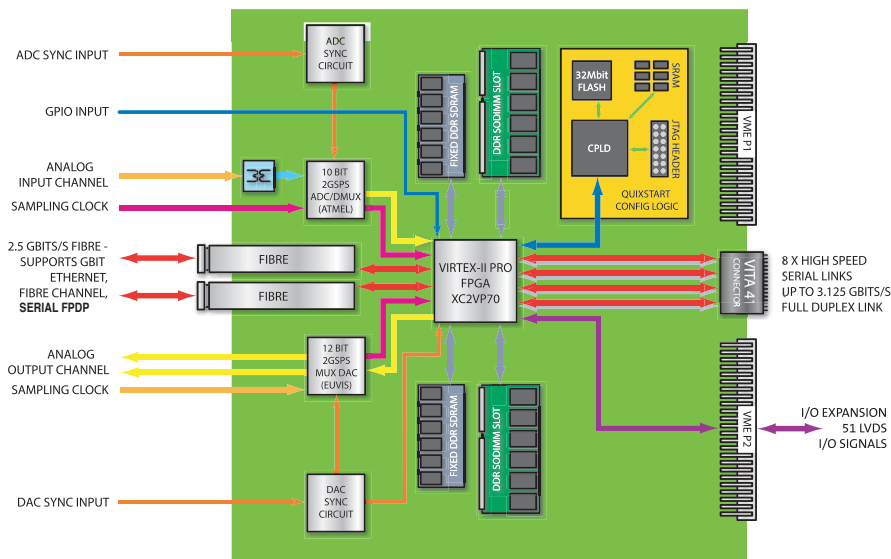
The Quixilica TRITON VXS-1 is part of the Quixilica VXS family of FPGA based processing hardware. The Quixilica VXS family provides a complete range of flexible analog and digital IO products in the VITA 41.0 VXS form factor. The product range couples high performance analog and digital IO front ends with a scalable FPGA based processing architecture. Memory and inter-processor communications resources have been optimized to address the requirements of very high performance real time digital signal processing applications. This family of products is supported by a series of development kits, FPGA cores and software, providing users with power and flexibility while retaining consistency and ease of use across the range. Key applications for the TRITON VXS-1 include radar, electronic warfare, software radio and telecommunications.

Hardware Description

The TRITON VXS-1 is a 6U form factor card that can be employed as a payload card as defined in the VITA 41.0 VXS

specification. The card can also be deployed in a standard VME 64 chassis if the P0 connector is not populated. The VME 64 interface is used only for powering the card - the VME bus interface itself is not implemented. Control and high speed data IO for the card will be implemented using the high speed serial links available on the front panel and/or the backplane P0 connector.

TRITON VXS-1 is supplied with a standard FPGA bitstream and Windows based software application for a single channel, snapshot data capture system and a single channel arbitrary waveform generator. A standard Gigabit Ethernet link to the front panel is used to interface to the host PC. A hardware reference manual provides users with sufficient detail to develop their own FPGA based applications. For rapid development, an additional Developers Kit can be purchased which contains FPGA interface cores, software and source code for the snapshot data capture system and arbitrary waveform generator as a reference design.



TRITON VXS-1 Block Diagram

FPGA

A Xilinx Virtex-II Pro XC2VP70 FPGA is at the heart of the TRITON VXS-1 product. The FPGA provides interfacing between the ADC, DAC, memories and IO resources on the card as well as providing the user with a platform for implementing high performance real time processing. The P70 FPGA provides two embedded PPC 405 processors and Rocket IO high speed serial multi GB/s transceivers. The Rocket IO links are the principal mechanism used for high speed data IO and control of the TRITON VXS-1 card.

Analog to Digital Converter

A 2 GS/s, 10 bit resolution analog to digital converter is provided on the TRITON VXS-1. The input channel is based around the Atmel AT84AS008 ADC part with a 1 to 4 demultiplexer chip. Build options for either an AC coupled, or a direct differential coupled analog input are available. A single ended clock input is provided for the ADC. The board can also be configured to use a single clock input common for both the ADC and DAC. The layout has been carefully designed to ensure phase matching in either clock configuration. A trigger input connection is provided on the front panel to allow the hardware to permit synchronization at sample level across multiple boards. A further general purpose input to the FPGA from the front panel permits additional system level control. Trigger firmware can be implemented in the FPGA for maximum flexibility.

Digital to Analog Converter

A 2 GS/s, 12 bit resolution digital to analog converter is provided on the TRITON VXS-1. The output channel is based around the EUVIS MD651D DAC, which includes a 4 to 1 input multiplexer. The output is AC coupled via a capacitor, and should be terminated in a 50 Ohm load. The DAC has either its own sampling clock input via a front-panel input or can share a common clock with the ADC. A

separate trigger input is also provided on the front-panel, directly into the FPGA to allow the user to synchronize multiple DAC outputs over a number of cards.

Memory

Two banks of onboard double data rate SDRAM memory are provided on the TRITON VXS-1 which is interfaced to the FPGA. DDR memory allows data to be read or written on both the rising and falling edges of the clock. Currently, 0.5 GBs per bank is provided with the memory arranged to have a 64 bit wide data bus. Deeper memories of up to 1 GB per bank will be offered in the future using higher capacity memory parts.

The TRITON VXS-1 also provides 2 independent SODIMM sites for Double Data Rate (DDR) SDRAM modules, interfaced to the FPGA. The SODIMM modules support 64 bit wide data transfers. Standard SODIMM modules up to 2 GB are available. Users can purchase their own modules or specify the memory they require as additional cost items to be fitted to the TRITON VXS-1 card prior to delivery.

Memory interface cores for the DDR memory are available for the FPGA as part of a Developer's Kit. These cores implement all of the complex memory control circuitry and provide the user with a simple FIFO style interface into their own application circuits in the FPGA.

Front Panel High Speed Serial IO

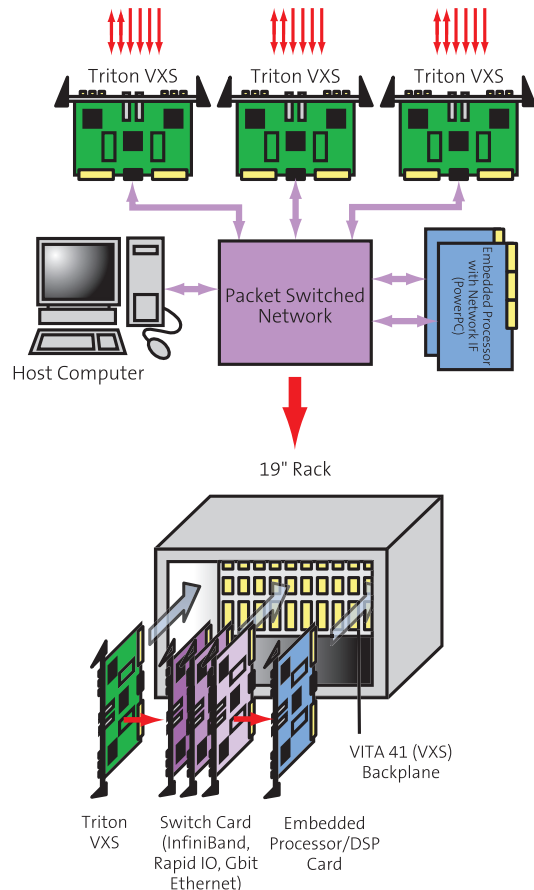
Two SFP sites are provided on the front panel of the TRITON VXS-1. These can be populated with commercially available fiber optic or copper SFP modules.

Alternative SFP modules for long wave fiber or copper (e.g. Gigabit Ethernet) can be supplied and fitted if required. Note: suitable FPGA cores are required to support the higher layers for specific protocols

The Quixtream over UDP FPGA cores and software is supplied as part of the Developer's Kit. This provides the user with a toolset to allow transfer of high speed data and control information between the FPGA and standard host computers running Windows or Linux via Gigabit Ethernet interfaces.

VXS Backplane High Speed Serial IO

The TRITON VXS-1 can be used as a VITA 41.0 payload card. Up to 8 high speed serial links of up to 3.125Gbit/s full duplex data rates are supported via the VITA 41.0 standard MultiGig RT2 P0 connector. Different custom or standard communication protocols can be run over these physical links by providing appropriate firmware in the FPGA.



Population of the VITA 41.0 P0 connector is a build option that must be specified if the user wishes to deploy the high speed serial links on a backplane. Other hardware and firmware products in the Quixilica range and from third party vendors are also available to aid rapid implementation of complete VXS systems. It is recommended that users should contact the factory to discuss their system requirements if they are considering using the high speed serial connections on the TRITON VXS-1.

P2 Connector GPIO

Up to 51 LVDS (2.5V) differential pairs from the FPGA are available on the P2 expansion connector. Sufficient information is supplied in the TRITON VXS-1 hardware manual for users to develop fully custom transition cards for their application if they need to do so. Tekmicro also has available a number of existing transition cards that are suitable for a wide range of simple GPIO applications. Customization for individual applications may be possible.

Quixstart FPGA Configuration

A number of options are available for configuring the FPGA on the TRITON VXS-1. For development purposes, a JTAG connection is available that allows users to configure the FPGA via standard Xilinx development tools such as Impact and Chipscope. When a stable design is available, an on board flash memory can be programmed with the final bitstream and the FPGA will configure on power up. QinetiQ's Quixstart configuration mechanism also supports flexible configuration or reconfiguration of the FPGA through a Gigabit Ethernet link. The TRITON VXS-1 can be set up to fetch its configuration from a remote server after a power up or reset event. This is useful for applications where different bitstreams may be used to run the board in different modes. It is also suitable for applications where remote bitstream reconfiguration is required or where it is undesirable to have bitstreams held in on-board flash due to security considerations.

The setup files and software required for the full Quixstart system are supplied as part of the Developer's Kit for the TRITON VXS-1.

Software Support

Basic Software

The TRITON VXS-1 is supplied with a bitstream and executable Windows GUI application for a single channel snapshot data capture system and single channel arbitrary waveform generator. The software allows captured data snapshots from the ADC to be read back to the host. It also allows samples for arbitrary waveforms to be downloaded to on-board memory for playback via the DAC. The design allows the DAC output to be fed back into the ADC for test purposes. This is intended to provide users with a mechanism to experiment with and verify correct operation of the card. To use the application, users will require a host PC equipped with a Windows 2000/XP operating system and a fibre optic Gigabit Ethernet interface.

A UCF file for the FPGA and a detailed hardware reference manual is provided to allow users to implement their own FPGA designs from scratch if desired.

Recommended Development Tools

The following development tools are required / recommended for use with the TRITON VXS-1 if users are developing their own FPGA designs for the card:

- Xilinx ISE or Foundation
- Xilinx Chipscope software (recommended for on chip hardware debugging)
- Xilinx Parallel IV JTAG download cable
- Simulation / Synthesis tools as preferred by the user. (If not using Xilinx Foundation)

- Xilinx EDK (Required if developing for embedded PPC 405 cores in FPGA)
- Microsoft Visual C++ (If using Application Developer's Kit)

TRITON VXS-1 Application Developer's Kit

To aid rapid development of user FPGA designs for the TRITON VXS-1, it is recommended that the additional Application Developer's Kit for the TRITON VXS-1 is purchased. This kit provides the following items:

- Quixilica Quixstream UDP/Gigabit Ethernet FPGA Cores host software (Windows and LINUX)
- DDR SDRAM FIFO Interface FPGA Cores
- Setup files and instructions for Quixstart FPGA configuration system
- Reference design - Source code for snapshot data capture system firmware and software, and for arbitrary waveform generator firmware and software.
- User manuals for all of the kit components and reference design

Signal Processing Cores

A complete range of high performance signal processing cores is available as part of the Quixilica family, including **floating point arithmetic, programmable FIR filters, Digital Receivers, FFTs and QR Decomposition**. Customization or development of IP for specific applications is also possible. Contact Tekmicro for availability of IP and targeted Application Developer's Kits for radar and EW applications using the the TRITON VXS-1.

Quixstream® Cores and Software for High Speed Interconnect

Tekmicro is continuing to develop support for other standard communications protocols as part of their Quixstream high speed communications product family. Contact us for availability of cores and software to support **InfiniBand, Serial FPDP** and more.

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Ordering Information

TRITON VXS-1 6U VME Digitizer Card
Part Number: Qx-TRITON-1-6-C-P-T-N

C = Signal coupling into ADC analog inputs
: B => AC coupled through balun transformer
: D => Direct differential inputs to ADC

P = P0 MultiGig RT2 Connector Build Option
: Y => Fit P0 Connector (For use in VXS Chassis)
: N => Don't Fit P0 Connector (For use in VME 64 Chassis)

Xilinx XC2VP70-6C Devices fitted as standard

T = Clock type
: I => Independent
: C => Coupled

Contact Tekmicro for following optional items:

- Alternative FPGA speed grades and/or industrial silicon variants
- Supply of DDR SODIMM modules pre-fitted
- Supply of copper or fibre SFP transceivers

TRITON VXS-1 Application Developers Kit

Part Number: Qx-TRI-DK01-DL

Contact factory for availability of additional DSP cores and Quixstream interconnect cores.



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