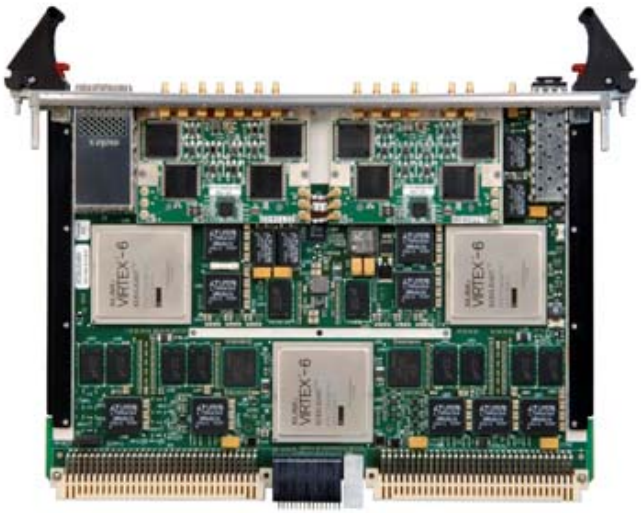
QuiXilica Digitizers Virtex-6 FPGA

The industry first QuiXilica-V6 VME/VXS FPGA board combines three Xilinx Virtex-6 FPGAs with two QuiXmodule sites, supporting the industry's widest range of Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) resolutions and bandwidths using a common hardware architecture.

Like previous generations of QuiXilica products based on the Xilinx Virtex family, the QuiXilica-V6 VME/VXS is compatible with legacy VME systems as well as newer ANSI/VITA 41 VXS based systems for both laboratory and deployed / rugged applications.



QuiXilica-V6 FPGA Density

The QuiXilica-V6 VME/VXS baseboard has three, highly connected, Xilinx Virtex 6 FPGA sites. The two front-end FPGAs are attached directly to the QuiXmodule sites, providing a simple and direct high speed connection between the ADC and DAC devices and the FPGA. The third FPGA can be used to support additional processing, and also any required protocol support for either front panel or backplane interfaces.

All of the FPGA sites use the FF1759 package, which supports both LXT devices, optimized for high density logic, as well as SXT devices, optimized for digital signal processing. Each of the three FPGA sites can support the devices shown in Table 1 below.

Table 1: QuiXilica-V6 FPGA Device Options

FPGA Device	Logic Slices	DSP Slices
LX240T-2	37,680	768
LX365T-2	56,880	576
LX550T-2	85,920	864
SX315T-2	49,200	1,344
SX475T-2	74,400	2,016

The options available with Xilinx Virtex 6 FPGA technology expand both the range of options and the maximum processing density, while improving both performance and power efficiency. Figure 1 shows the relative logic and DSP processing capability for the QuiXilica-V5 family, a higher density Virtex 5 based option, and the QuiXilica-V6 VME/VXS baseboard. The QuiXilica options are shown in both minimum and maximum FPGA density configurations.

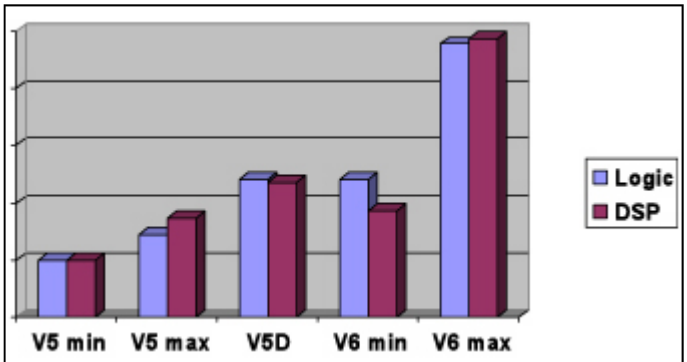


Figure 1: Processing Capability in FPGA Processing Board

The options available with Xilinx Virtex 6 FPGA technology expand both the range of options and the maximum processing density, while improving both performance and power efficiency. Figure 1 below shows the relative logic and DSP processing capability for the QuiXilica-V5 family, a higher density Virtex 5 based option, and the QuiXilica-V6 VME/VXS baseboard. The QuiXilica options are shown in both minimum and maximum FPGA density configurations.

Memory Resources

QuiXilica-V6 includes six banks of DDR3 memory with total capacity of 5 GB (with future options for 10 GB) and aggregate throughput of 32+ GB/s, supporting a wide range of signal processing algorithms with deep memory buffering of the entire signal acquisition stream. The back end FPGA also supports two banks of QDR II+ memory for additional flexibility.

Network Interconnect

The QuiXilica-V6 VME/VXS baseboard provides a rich set of network interconnect options for both control and data plane communications. An onboard Gigabit Ethernet switch provides an integrated LAN-on-board network which connects the front panel interface, backplane interfaces, FPGA nodes, and system management processor into a local area network for control and status monitoring. The VXS backplane fabric interface can also support dual 10 Gigabit Ethernet interconnect using 10GBASE-KX4 interfaces with appropriate protocol cores in the back end FPGA.

Serial Interconnect

The QuiXilica-V6 VME/VXS baseboard supports 12 full duplex high speed fiber optic connections through the front panel along with 8 to 12 full duplex high speed fabric connections through the VXS P0 connector. Each Virtex 6 GTX transceiver supports up to 6.4 Gbps using either 8B/10B or 64/66 encoding, increasing the effective data rate by almost 2.5x per link over Virtex 5 GTP based solutions. When all front panel and backplane links are utilized, the QuiXilica-V6 VME/VXS baseboard supports total aggregate bandwidth of 37 GB/s (18.5 GB/s in each direction) to other off board processing resources. With suitable IP cores instantiated in the user's application firmware code, a wide range of standard communication protocols accross the high speed serial physical layer can be supported, including PCI Express, Serial FPDP, 1 and 10 Gigabit Ethernet and Aurora.

System Management

The QuiXilica-V6 architecture incorporates a next generation system management processor for bitstream management, board sanitization, power and thermal monitoring, built-in-test and extended diagnostics. The system management processor supports both I2C and Gigabit Ethernet interfaces to support both VITA-46.11-style system management as well as network-based protocols. All system management functions may also be accessed through the VMEbus interface for legacy applications that require a VME-based control architecture.

Ruggedization Support for Deployed Applications

All QuiXilica-V6 VME/VXS products are available for a wide range of operating environments, including commercial grade, rugged air and conduction cooled, allowing the card to be used for both laboratory and deployed requirements in both VME and VXS systems.

Comprehensive Developers Kit Speeds Time To Market

All QuiXilica-V6 products are supported by a comprehensive Developer's Kit that includes interface IP cores for all onboard resources along with Tekmicro's QuiXtream network toolkit for rapid application development using network-enabled FPGAs. Reference designs are included, with source code, to support quick prototyping of user applications with minimal learning curve. The QuiXilica-V6 Developer's Kit maintains common APIs across FPGA families, supporting rapid, easy migration of existing V5 applications to V6 technology.