FPGAs and VITA 41 address mil sensor processing design challenges

By Andrew Reddig

Military sensors for applications, such as radar and sonar, spew enough data to overwhelm most systems. Not only must the data be collected at the front end, but also it must be moved into and around the system and digitally signal processed before it is of any value. The challenges of aggregating the data at the front end, processing it, and finally distributing it are considerably eased by using parallel processing in FPGAs. Additionally, new open VME standards, for instance VITA 41, support multi-gigabyte serial communications schemes such as RapidIO, InfiniBand, Ethernet, and PCI Express, while offering new architectures for in-line processing and multiprocessing.

Meeting the needs of the latest military sensor requirements is creating problems for current system designers. Due to increasing computational requirements, engineers are being forced to look at alternative processing strategies. One well established processing option is to use Field Programmable Gate Arrays (FPGAs), which provide higher density computation rates compared to DSPs or CPUs. Yet, FPGAs are not able to completely solve the problem. In many cases, the computational requirements are either too high for a single processing node or VME card, or demand heterogeneous system implementation using combinations of processors.

Such implementations need high-density computation and a methodology to combine the processing nodes using high-bandwidth interconnects. Current VME-based systems are unable to provide the required bandwidth. However, the VITA 41 VXS standard, when combined with the latest FPGA technology, is able to provide an answer to this problem.

The VITA 41 standard specifies a high-bandwidth, switched-fabric communications architecture with mechanical and electrical compatibility with VME64. It enables the development of scalable processing solutions to meet the challenges of modern military sensor processing systems. FPGAs are an ideal technology for a wide range of signal processing operations found in these systems. They combine the capability for very high-performance digital signal processing, with multiple high-speed serial communications interfaces to support the equally high data bandwidths required for current military sensors. There is a growing ecosystem of vendors supporting the VITA 41 standard with chassis, switches, digital and analog I/O, CPU-based processing, and FPGA-based processing and switching cards.

The challenges

Designers of military sensor and signal processing systems, such as radar, communications, and electronic warfare, face an increasingly difficult set of challenges. These challenges include:

- Detecting smaller targets at longer range
- Detecting targets within clutter and countermeasures
- Accurately identifying targets, all within the real-time constraints of a military engagement

These requirements drive the development of ever more complex signal and data processing algorithms. This, in turn, demands that processing performance spiral upward. At the same time, the physical constraints placed on the designer can be very demanding. For example, a sensor designed to be deployed in an Unmanned Aerial Vehicle will be severely constrained by the available size, weight, and power budgets. The two contradictory requirements – increasing levels of performance within a smaller physical envelope – are now forcing designers to consider a range of implementation technologies to supplement conventional microprocessors or digital signal processors.

The drive to more complex algorithms is also being fuelled by advances in sensor and data acquisition technologies. For example, the AT84AS008 A/D converter from Atmel digitizes at a rate up to 2.2 GSps at 10 bits, providing the capability to process approximately 1 GHz of signal bandwidth directly in the digital domain. This can considerably simplify the analog RF blocks of a system architecture, potentially removing the need for one or more stages of analog down-conversion. Alternatively, it can remove the need to segment the signal bandwidth into a number of frequency channels, each of which must be processed by separate analog and digital blocks. It also offers the possibility of implementing new and more complex algorithms, for example, broadband rather than narrowband radar beam-forming. However, these benefits come at the cost of making the digital signal processing more complex because it must accommodate a data stream on the order of 2 GSps per receiver channel.

With a typical deployed VME system in an ATR chassis, the application size, weight, and power considerations will drive the designer to maximize the number of analog signal channels digitized in each payload slot. For example, digitizers available from a number of vendors implement two 10-bit, 2 GSps AD converter channels, which provide an aggregate data bandwidth into the digital signal processing of 40 Gbps from each digitizer card. This presents a significant challenge to the system architect to provide a communications infrastructure that can support the aggregate data rates present in multichannel radar and communications sensors. VITA 41, with its serial switched architecture, provides a way to move all of this data around a sensor processing system.

VITA 41 technology solutions

VITA 41 is an open standard with a growing ecosystem of product vendors (for a list of current vendors, see the April 2005 issue of *VMEbus Systems*). The design engineer has a growing choice of interoperable, Commercial Off-The-Shelf (COTS) components with which to design sensor processing systems.

VITA 41, also known as VXS (VME switched serial), is the latest evolution of the VME standard. It provides a switched fabric of high-speed serial connections in addition to a full implementation of the VME64 backplane standard. A VITA 41 chassis contains a number of payload slots and switch slots as shown in Figure 1, per the VITA 41.0-200x, Rev 1.10, September 2004 specification. Each payload slot has eight 3.125 Gbps serial channels, providing an aggregate data bandwidth of 2.5 GBps (enabling 8B/10B encoding) in and out of the slot in full-duplex mode.

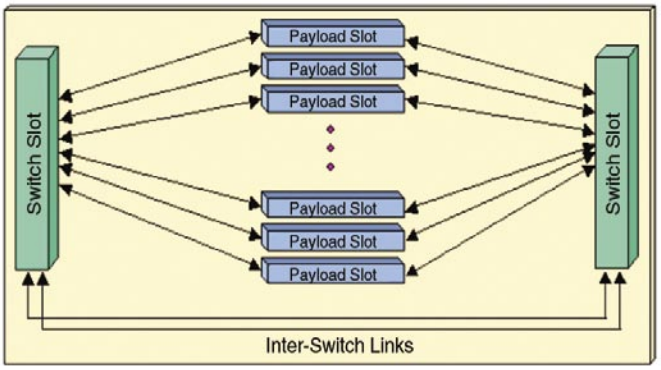

Figure 1

The switch slots each support 76 serial channels, connected via the backplane to the payload slots, and provide an aggregate full-duplex data bandwidth of 190 GBps (after 8B/10B encoding) in and out of each switch slot. All channels can operate concurrently, enabling multiple simultaneous communications between switch and payload slots. This configuration greatly increases overall system bandwidth compared with a bused architecture such as VME64, giving the designer considerable flexibility for specifying the timing of data transfers within the architecture.

VITA 41 also specifies a number of interconnect standards, defining how a number of standard, open, high-speed serial communications protocols are implemented on the VITA 41 architecture. Table 1 lists the standards that are published or in preparation.

Protocol	Standard
VITA 41.1	InfiniBand
VITA 41.2	Serial RapidIO
VITA 41.3	Gigabit Ethernet
VITA 41.4	PCI Express
VITA 41.5	Aurora

Table 1

Sensor processing architectures

The latest generation of FPGAs provides not only a platform for high-density computation but also support for the high-performance features of VITA 41, and enables the design of sensor processing systems with low Size, Weight, and Power (SWAP) as well. For example, the Xilinx Virtex-II Pro FPGA family includes devices with up to 16 or 20 Multi-Gigabit Transceivers (MGTs), which are compatible with the high-speed serial signals used in VITA 41. The MGTs can support a variety of open communication standards including GigE, InfiniBand, Fibre Channel, and serial FPDP. This feature provides the designer with the flexibility to interface the FPGA to a wide range of external devices. For example, the FPGA can input data directly from a sensor that uses serial FPDP; it can stream sensor data to a RAID array using Fibre Channel; or it can connect directly to a host PC using GigE and UDP/IP or TCP/IP for control and user interaction.

The biggest benefit of using FPGAs in sensor processing systems is their ability to implement regular signal processing functions very efficiently and with very high performance. FPGAs achieve this by implementing many arithmetic operators in parallel on a single device. For example, the Quixilica QR decomposition core from QinetiQ can be implemented in excess of 140 floating-point arithmetic operators (a mixture of adder/subtractors, multipliers, and dividers), and the core can be clocked at speeds in excess of 150 MHz, providing a sustained arithmetic rate of more than 20 GFLOPS while dissipating approximately 25 W.

By comparison, the performance of an Intel Pentium CPU implementing the same algorithm was 4 GFLOPS at 70 W. The challenge with FPGA designs of this type is the design of efficient control and data scheduling to ensure that each arithmetic operator carries out a useful operation on every clock cycle. However, once an efficient design has been achieved for a particular signal processing function, it can be encapsulated as an IP core, which can be reused in many designs. There are many vendors offering IP cores to implement a wide range of DSP building blocks.

Fortunately, the front-end signal processing functions typical of the front end of many sensor processing systems lend themselves ideally to implementation in an FPGA. They are characterized by relatively simple control structures, highly repetitive arithmetic operations, and, in many cases, relatively little storage of intermediate results. FIR filtering, digital down-conversion, and FFTs are good examples of this type of operation. In a recent application, which made extensive use of FFTs to analyze the spectrum of multichannel sensor data, the FFT was ported from a conventional CPU-based architecture (using VME 64-based quad-PowerPC cards) to a VITA 41 FPGA-based architecture. In this application, the FPGA was located on the same card as the ADCs, which digitized the analog sensor data. It was possible to implement all of the FFT-intensive preprocessing on a single FPGA, eliminating 10 quad-PowerPC cards from the system.

Application example

To illustrate the benefits of VITA 41 and FPGAs for implementing sensor processing systems, consider the following example of a phased-array, radar-adaptive beam-forming application, as shown in Figure 2. The system uses four antenna channels, with analog receiver and down-conversion providing an intermediate frequency of 1 GHz bandwidth. This data is digitized directly using four 10-bit, 2 GSps ADCs, located on two VITA 41 payload cards. Each ADC produces a data rate of 20 Gbps, so the aggregate data rate for the pair of channels on a payload card is 40 Gbps or 5 GBps, orders of magnitude greater than current VME systems can support, but only twice the available VXS bandwidth of the payload slot. It is, therefore, necessary to reduce the data rate by preprocessing the data on the payload card. This is done within an FPGA on each digitizer card. In this case, the preprocessing consists of digital down-conversion, followed by decimation in the data rate by a factor of 8, which reduces the data rate to 5 Gbps, within the VXS payload bandwidth.

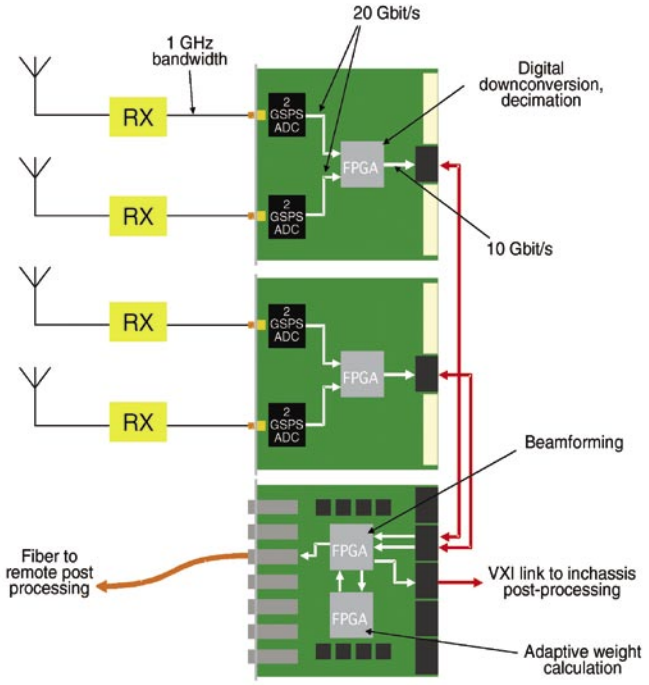

Figure 2

The channel data is transmitted to an FPGA-based processing card located in the VXS switch slot. Here, the data from all four channels is combined using adaptive beam-forming. The beam-forming operation is a simple spatial filter – a set of complex multipliers followed by an adder tree. The adaptive coefficient calculation is carried out using QR decomposition, with the channel data being buffered in memory while the coefficients are calculated. The switch slot is an ideal position in the VXS architecture in which to implement the beam-forming operation, because beam-forming requires data from all of the channels. The adaptive weight calculation operation is highly computationally intensive. However, using an FPGA-based processor in the switch slot enables the operation to be carried out within a single card, removing the need to distribute the algorithm and data across an array of CPU or DSP cards. This configuration, in turn, considerably simplifies the system architecture.

The adaptive weight calculation is implemented in a single FPGA, with the coefficients passed to a second FPGA in order to apply them in the beam-former. The whole architecture is highly scalable, and more antenna channels can be added to improve the beam-forming capability, which will increase target detection and interference rejection capability. Additional digitizer cards may be added to the system, with the VXS backplane supporting up to 18 payload cards.

Within the front-end preprocessing as just described, the high-speed serial interconnections across the VXS backplane are implemented using Aurora, a lightweight, open protocol developed by Xilinx. These interconnections are possible because both ends of the communication links utilize the FPGAs, therefore remain under the control of the developer. The output from the front-end preprocessing, consisting of one or more data streams representing spatially formed beams, is transmitted to other subsystems for subsequent processing using a standard protocol such as InfiniBand. This setup takes advantage of standard, commercially available networking components.

Self-contained sensor processing

Military sensors will continue to require the latest processing and interconnection strategies to meet an ever-increasing processing burden. Thus, algorithm complexity and processing intensity will continue to increase. However, with standards such as VITA 41, a new range of development options is now available to the designer. The combination of FPGAs and high-bandwidth interconnections enabled through VITA 41 can provide solutions to system requirements that previously were considered unfeasible.

Quixilica VXS cards from QinetiQ are examples of VITA 41 FPGA cards. One possible implementation of the application example described earlier uses the Quixilica Neptune VXS-1 digitizer and the Callisto VXS-1 processing and switch cards from the architecture in Figure 2. Neptune provides two 2-GSps 10-bit digitizer channels, with a Virtex-II Pro P70 FPGA and DDR memory, and Callisto (Figure 3) implements five Virtex-II Pro P50 FPGAs, each with DDR SDRAM. In the example architecture, and by using high-bandwidth interconnection protocols such as Xilinx Aurora, data distribution of the required processing chain can be made to the appropriate FPGA processing platform such as from Neptune to Callisto. Using FPGA technology not only makes the system feasible but also significantly reduces the SWAP compared to architectures based around DSPs or CPUs.

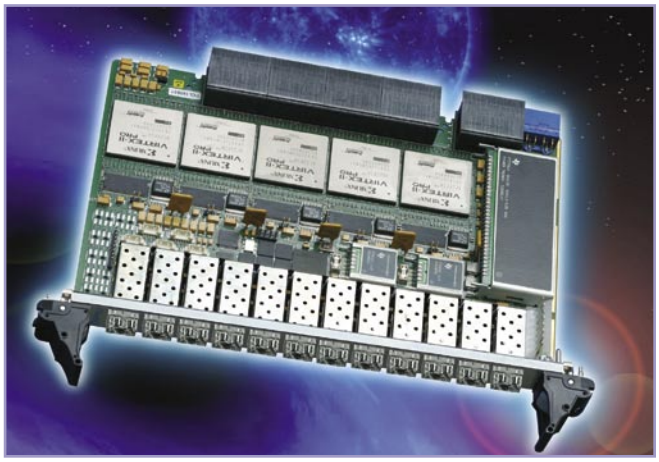

Figure 3

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